TECHNOLOGY WHITE PAPER

The Power Architecture® QorIQ™ Platforms: Architectural Benefits for Small Form Factor Embedded Applications

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Introduction

Today's embedded, aerospace and defense industries rely heavily on modern, embedded technology solutions that cater to the power, size, and performance requirements needed for mission-critical systems. For over 20 years, Freescale™ Power Architecture microprocessors have provided reliable, scalable processing options to suppliers of Single Board Computers (SBCs) used in embedded compute-intensive applications. Power Architecture's adoption of multicore processing technology and virtualization in the last 6 years, as well as its support for legacy upgrades, has further strengthened its reputation as a leader in processor innovation.

The Power Architecture QorIQ family of System on a Chip (SoC) platforms, introduced by Freescale in 2008, offers designers a range of advanced SOCs, with different levels of performance, power, cost and programmability in a compact package. Curtiss-Wright is using QorIQ SOCs to meet the size, weight, and power demands of embedded electronics on the 3U Power Architecture VPX3-131 and VPX3-133 SBCs, maximizing performance and functionality while minimizing power. Through the P4080 used in the VPX3-131, and the T2080 used in the VPX3-133, this white paper will illustrate why Power Architecture continues to be an excellent choice for use in small form factor embedded applications.

Designing Embedded Systems: Why Power Architecture?

In embedded, aerospace and defense applications, many important factors such as performance, power dissipation, data protection, and scalability come into play when selecting appropriate processors for deployed embedded electronics. Power Architecture technology continues to address these key characteristics by providing an optimized balance of performance and power along with ensuring long-term program investment.

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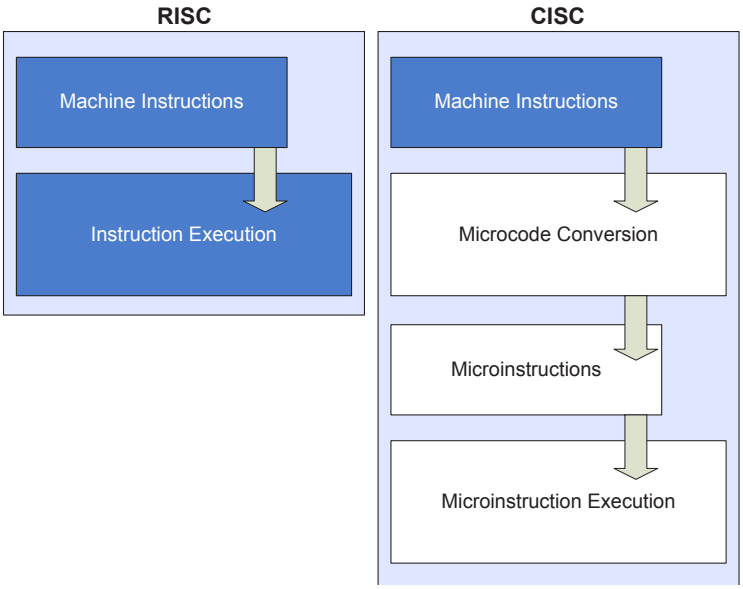

Figure 1: RISC vs. CISC

RISC architecture: power efficient and cost effective

Power Architecture is a RISC architecture (Reduced Instruction Set Computing), using a simplified instruction set that requires fewer microprocessor cycles per instruction than CISC (Complex Instruction Set Computing) or VLIW (Variable Length Instruction Word) alternatives. The simplified nature of RISC also results in a lower transistor count than its competitors - for example, 90 million transistors for a typical Power Architecture chip vs. 1+ billion transistors for a CISC architecture Intel x86 processor.

The combination of fewer cycles per instruction and a lower transistor count allows RISC to deliver a superior MIPS (Million Instruction per Second) to watt ratio, allowing processors to operate on significantly less power. The lower transistor count also results in reduced manufacturing costs compared to chips using alternative architectures.

The benefit for Power Architecture-based processors is that they produce cost effective, power efficient, high performance data compute solutions, making them ideal choices for SWaP-constrained embedded applications.

Determinism and power dissipation

One of Power Architecture's most well-known characteristics is its determinism, the ability to execute an operation on a given data set within a defined and consistent time interval. Compare this with the temperature-driven variations in x86 processor operation caused by throttling. Throttling is defined as the slowing down of core clock frequency, resulting in reduced system performance. This occurs in x86 processors when the core temperature reaches a pre-determined value and the core clock will not return to its normal frequency until the unit has sufficiently cooled. The clock frequency can also fluctuate over time as the core temperature heats then cools, and heats again, resulting in un-predictable performance. Rugged embedded applications generally operate with real time requirements and cannot cope well with slowing or sub-par performance due to overheating and throttling.

Unlike industry competitors such as Intel, where processor throttling continues to be an issue in all types of platforms from desktop PCs to embedded systems, Power Architecture processors do not allow throttling, no matter how overheated they become. However, that does not mean that Power Architecture ignores power dissipation issues. In fact, it offers many power-saving features, such as power-gating, and software-selectable power-saving modes that reduce function in certain areas when idle and provide excellent energy management.

Power Architecture's handling of power dissipation is of paramount importance in high performance, small form factor embedded solutions that require deterministic performance, and results in not only the lowest possible power consumption, but reliable, consistent processor performance on both the hardware and application levels.

Safety certification

As the complexities of embedded solutions grow, safety certification has become an increasingly necessary step to ensure the security of deployed systems. The purpose of safety certification is to provide guidelines for the design and documentation of safety-critical embedded systems to confirm they will perform with a required level of confidence in their safety. DO-178C and DO-254 are two examples of internationally recognized safety certifications. Because of their deterministic execution qualities, simplified RISC instruction set, and Freescale's openness and willingness to support certification requirements, Power Architecture processors are the leading choice for those seeking safety certification.

Scalable, integrated solution

Today's systems not only rely on the MIPS per watt ratio to determine a processor's efficiency, but also take into account the degree of integration as an indicator of overall performance. Implementing communications subsystems such as Ethernet controllers, PCI Express® (PCIe) interfaces, memory controllers and on-chip caches with error protection and correction provide greater performance and reliability improvements over less integrated counterparts.

In addition to a high level of integration, Power Architecture also offers software scalability. With very long service lives, military platforms require solutions that can be scaled and upgraded over the years without having to invest heavily in an entirely new system. Power Architecture vendors such as Curtiss-Wright strive for software compatibility across their Power Architecture platforms. This makes it very easy for buyers to scale their platforms over time, and ensures long-term program investment protection.

System on a Chip: Freescale's Power Architecture QorIQ Processors

In 2008, Freescale released its QorIQ line of communication microprocessors. Designed with networking in mind, and enabling new levels of programmability and performance with multiple core architectures, QorIQ microprocessors utilize Freescale's Power Architecture technology and also, more recently, ARM-based technology. The QorIQ brand is segmented into product families based on functionality and performance, with each offering unique architectural features that make QorIQ products adaptable and versatile for use in many types of applications.

Each QorIQ microprocessor is a System on a Chip (SoC) that combines the embedded processor, memory controllers, timing sources, USB and Ethernet controllers, power management circuits, DMA controllers, flexible SerDes and software, allowing one chip to perform all the functionality that previously required several devices. This integration provides many benefits such as:

- lower power
- higher performance
- improved efficiency
- lower overall manufacturing cost
- simplified board design
- greater system reliability
- smaller footprint required for small form factor applications

SoCs are used in a variety of applications, including SBCs, Digital Signal Processors, Video Decoders, mobile phones, and portable media devices. Because of the many core options available, Freescale's QorIQ SoC platforms also provide a multicore migration solution that easily allows users to upgrade to more cores as they see fit.[1]

The P4080 processor

The P4080 is a member of QorIQ's P Series family and, when released, quickly became the leading product of the QorIQ line.[2] The P4080 is highly integrated and designed with performance and power in mind, giving it versatility in a wide range of applications. It can be used for datapath, control, and application layer processing, all performed by one unit of silicon. A combination of high performance and a high level of functional integration make it ideal for supporting compute-intensive applications within the limited space of the 3U form factor.[3]

Figure 2: Freescale's P4080 processor

The P4080 features 8 Power Architecture e500mc cores operating up to 1.5 GHz that provide high performance datapath acceleration logic, as well as integrating the peripheral and network bus interfaces used in embedded applications. Integrated interfaces include dual 64-bit DDR3 SDRAM memory controllers supporting up to 64 GB of memory, plenty of cache, and an embedded hardware Hypervisor to ensure multiple software systems can run efficiently on multiple cores concurrently with high integrity. In addition, advanced virtualization capabilities allow each core to run fully independently of the others, ensuring the safe operation of multiple operating systems. In combination, these features provide applications with a very high performance data flow in a SWaP-optimized footprint.

For I/O flexibility, the P4080 provides 16 configurable SerDes lanes. These can be configured to support 10/100/1000-BT Ethernet, 10 Gigabit Ethernet, PCIe or Serial RapidIO® (SRIO) ports. The P4080 may have any combinations of up to 4 PCIe controllers, 2 SRIO controllers, and 8 Ethernet controllers. It also incorporates datapath and crypto-acceleration units to streamline the processing of data.

The T2080 processor

The T2080 is a member of QorIQ's T Series family. It excels as a datapath, control, and application layer processor and is well-suited to the size, weight, and power needs of 3U compute-intensive embedded applications.

The T2080 features a processor cluster of 4 dual-threaded e6500 64 bit cores, each equipped with an AltiVec™ vector processing unit, all with a shared 2 MB L2 cache and operating up to 1.8 GHz. A single 32/64-bit DDR3/3L SDRAM memory controller with ECC is provided with a 512 KB platform cache. Like the P4080, the T2080 uses an embedded hardware Hypervisor and virtualization to allow each core to run independently of the others, enabling multiple operating systems to safely function together.

The T2080's AltiVec unit is a 128-bit vector Single Instruction Multiple Data (SIMD) processing engine available in previous generation Freescale processors such as the MPC7447A and 7448. The AltiVec vector processor unit allows the processor to work on multiple units of data with each instruction cycle, and consequently dramatically accelerates the execution of many certain algorithmic-intensive computations. For applications that are using AltiVec in SBCs with older AltiVec-equipped devices, such as the 7447A and 7448, this is an ideal upgrade path. Because the AltiVec unit and its vector commands are the same, algorithm software can migrate easily to the T2080.

For I/O flexibility, the T2080 provides 16 configurable SerDes lanes. These can be configured to support 10/100/1000-BT Ethernet, 10 Gigabit Ethernet, PCIe or SRIO ports. The T2080 may have any combination of up to 4 PCIe controllers, 2 SRIO, 2 SATA 2.0 and up to 8 Ethernet controllers. Like the P4080, the T2080 also incorporates datapath and crypto-acceleration units to accelerate processing of data.

Trust Architecture

In a world where security threats are constantly on the rise, protecting sensitive data and controlling access to sensitive systems are high priority concerns. Power Architecture is a leader in secure computing and provides many features that allow developers to create secure systems.

Freescale's Trust Architecture provides customers with a method of protecting their IP as well as ensuring that application code running on their SBCs is "trusted" (i.e. it is what is supposed to be executed and has not been

modified). Salient features of the Trust Architecture are Secure Boot, an embedded Hypervisor, Peripheral Access Management Units (PAMUs), Internal Boot ROM, Secure Fuse Processor, security monitor and Run Time Integrity Checker.[4]

Secure Boot

Secure Boot is one cornerstone of QorIQ's Trust Architecture. This process allows system designers to ensure that a system image can be trusted (i.e. it was created by a trusted source) before it is loaded. This is accomplished by "signing" the load using a public and a private key, and then verifying the signature prior to execution. Loads can also be encrypted for added protection. Secure Boot executes security health checks and verifies the authenticity of digital signatures using internal boot code that cannot be tampered with. Secure Boot not only prevents the processor from running arbitrary code, but also prevents attackers from extracting sensitive values, and prevents the modification of security and other device configurations.[5]

Memory Management Unit (MMU) and hardware Hypervisor

Multicore processors require functionality to ensure that the multiple cores and multiple operating systems work properly together. Each core is equipped with its own Memory Management Unit (MMU) whose job it is to distinguish the address ranges that a core is allowed to access. Each core can be configured to have access only to certain resources. To facilitate the partitioning of multicore SoCs, and increase resiliency against unauthorized accesses, a hardware Hypervisor helps control access between the multiple operating systems and the cores. In addition, if malicious software attempts to access and/or overwrite configurations, the Hypervisor blocks it.

Peripheral Access Management Unit (PAMU)

While the Hypervisor protects unauthorized software access, the CPU's internal components also require protection from malicious read/write attempts. The Peripheral Access Management Unit (PAMU) is equipped with address translation capabilities, and controls access to all bus components of the system. PAMU's access control may be configured as absolute or conditional.

Secure debug controller

The integrated nature of SoCs results in a simplified board layout as well as the elimination of external buses. As developers may have concerns about debug visibility in SoCs, Freescale developed secure debug architecture with features such as performance monitoring registers in both core and platform, run control, high speed trace port, and data acquisition trace. These capabilities afford developers the confidence they need in preventing unwanted interactions between CPUs.

SEC 4.0/5.2 Run Time Integrity Checker and session key storage

SEC 4.0 and 5.2 are Freescale's 4th and 5th Generation crypto-acceleration engines. SEC 4.0 is used on the P4080 while SEC 5.2 is used on the T2080. In addition to header and trailer processing and encryption checking, SEC 4.0 and SEC 5.2 are part of Power Architecture's Trust Architecture. This enables SEC 4.0 and 5.2 to aid in Secure Boot and perform runtime code integrity checks.

As QorIQ products may produce more session keys than can be stored in the processor's memory, SEC 4.0 and 5.2 also supports the encryption of session keys, which can then be stored in off-chip memory, and decrypted as needed.

Tamper detection

QorIQ's Trust Architecture provides the option for an OEM to set awareness mechanisms that detect physical contact with the processor. Some of these alerts can be programmed on switches (for example, notifying the user if the enclosure has been opened or the heatsink has been removed), sensors (for example, voltage or temperature) and in fiber-optic mesh surfaces. The architecture also provides for real time integrity checking of data stored in memory to detect tampering of the data during execution.

The QorIQ Advantage In Motion: Curtiss-Wright's 3U Power Architecture SBCs

Curtiss-Wright expertly addresses the need of 3U applications in the embedded, aerospace and defense markets by incorporating the high performance, high security advantages of the QorIQ SoCs into industry-leading 3U OpenVPX™ SBCs.

The 3U OpenVPX VPX3-131 SBC

The VPX3-131 is a general purpose, rugged 3U OpenVPX single board computer (SBC) featuring Freescale's octal-core QorIQ P4080 Power Architecture processor operating at 1.2 GHz. The VPX3-131 is designed to accommodate not only the P4080, but the single/dual core P5020/5010 and the quad core P3041. With 8 lanes of configurable backplane PCIe Gen2 fabric, two 10/100/1000 Ethernet ports, a single XMC site, 8 GB DDR3 SDRAM, 256 MB NOR flash, and support for 8 different OpenVPX slot profiles, the VPX3-131 combines the performance and advanced I/O capabilities of Freescale's QorIQ 64-bit processors with an extensive set of advanced I/O that provides a powerful processing solution for SWaP-constrained environments. It delivers a high level of computing functionality in a small 3U form factor with very low power requirements relative to its level of processing performance, while at the same time providing industry-leading I/O flexibility.

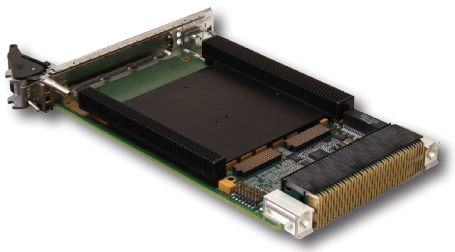

Figure 3: 3U OpenVPX VPX3-131 SBC

The VPX3-131 is Trusted COTS™-enabled. It uses the industry-leading benefits of the P4080's Trust Architecture for secure, uncompromised computing. It is software-compatible with Curtiss-Wright's VME-186 and VPX6-187 SBCs, supporting the transfer of applications from these SBCs into 3U VPX form factor systems.

The VPX3-131 is an excellent choice for use in high performance sensor processing applications, and for systems requiring a path to safety certification. DO-178C certifiable BSPs are available for several Curtiss-Wright Power Architecture SBCs. Contact Curtiss-Wright for further information.

The 3U OpenVPX VPX3-133 SBC

The VPX3-133 is a rugged 3U OpenVPX single board computer (SBC) featuring Freescale's quad-core QorIQ T2080 Power Architecture processor operating at 1.5 GHz. The VPX3-133 includes 8 lanes of configurable backplane PCIe fabric, 8 GB DDR3 SDRAM, two 10/100/1000 Ethernet ports, 256 MB NOR flash, 8 GB NAND flash, a single XMC site, and support for 8 different OpenVPX profiles. It combines the performance and the advanced I/O capabilities of Freescale's QorIQ dual-threaded quad core Altivec-equipped 64-bit processor with an extensive set of I/O that provides an extremely powerful processing solution for SWaP-constrained environments. It delivers high performance computing in a small 3U form factor with only 40 watts (maximum) of power while providing industry leading I/O flexibility.

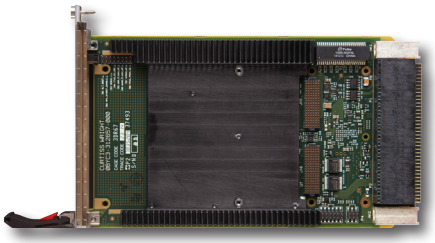

Figure 4: 3U OpenVPX VPX3-133 SBC

Like the VPX3-131, the VPX3-133 is Trusted COTS-enabled and includes all the benefits of QorIQ's T2080 Trust Architecture. With a leading MIPS to watts ratio, the VPX3-133 is an ideal choice for applications where maximum amounts of processing is key, or where consolidating multiple applications onto a single processor is required.

Application Examples

The VPX3-131 and VPX3-133 are well suited for a variety of applications. The following diagrams show some examples of typical system configurations with other Curtiss-Wright resources.

Configuration 1: Mission computer for rotary wing and fixed wing application

This architecture provides for a very powerful mission computer with support for multiple high speed graphics heads provided by Curtiss-Wright's VPX3-716 3U graphics cards, all powered by the Power Architecture VPX3-131. Each VPX3-131 can accommodate mezzanine cards such as 1553, ARINC 429, or FPGAs, and the VPX3-716s can accommodate mezzanines as well. This system configuration delivers maximum power in a minimal footprint.

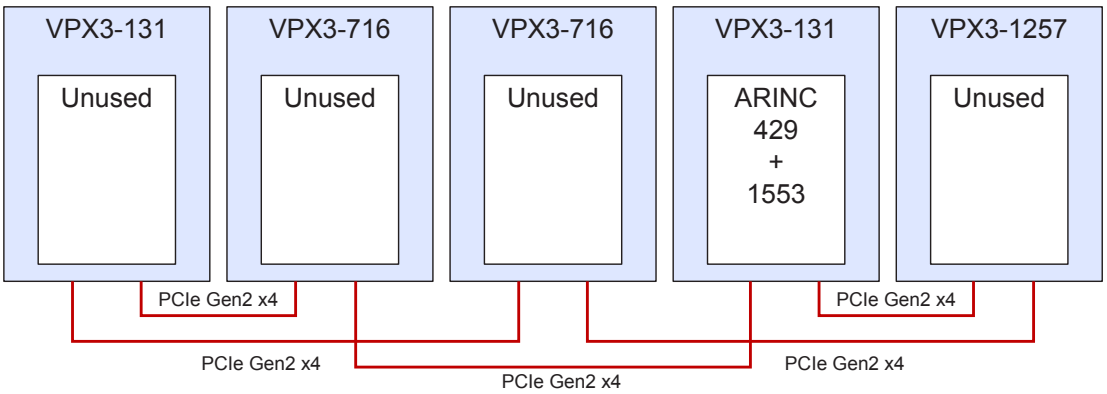

Figure 5: System design for a mission computer for rotary wing and fixed wing application

Configuration 2: High performance sensor processing

Note: The following configuration could be implemented with either the VPX3-131 or the VPX3-133.

This example illustrates a potent ISR mission computer, with Curtiss-Wright's FPGA05 cards being used to capture and process collected data, and additional processing done using the T2080's four AltiVec engines in each VPX3-133. A third VPX3-133 is used for I/O control. This configuration is designed to meet the challenge of high-density computing by providing an impressive amount of processing performance with the greatest functionality in a small, low-powered footprint.

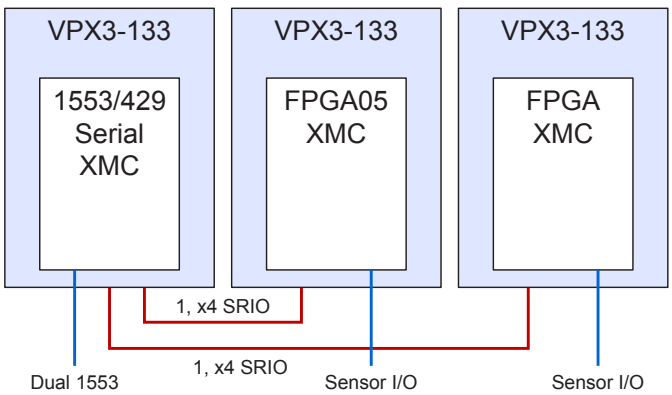

Figure 6: High performance sensor processing

Configuration 3: SWaP-optimized dual-head accelerated graphics

The example below illustrates a small mission computer controlled by the 4 high speed cores of the T2080 on the VPX3-133 along with the 3U VPX3-716 graphics card. This architecture provides the application with high performance, AltiVec-enhanced processing ideal for SWaP-constrained graphics-intensive applications.

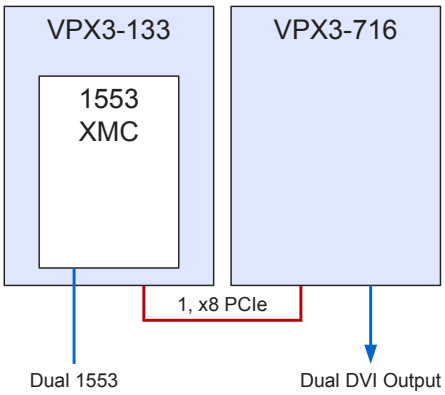

Figure 7: SWaP-optimized dual-head accelerated graphics

3U Power Architecture Systems: Tried, Tested and True

Power Architecture's proven adaptability and reliability over two decades of high performance solutions has solidified its place in today's aerospace and defense embedded market. The QorIQ SoC technology has advanced the capabilities for small form factor applications in SWaP- constrained environments, maximizing performance and efficiency while lowering power requirements and cost. Curtiss-Wright is committed to offering the latest SWaP-optimized Power Architecture technology in our SBCs, meeting the needs of most embedded applications. Contact Curtiss-Wright today to find out how you can use Power Architecture's QorIQ technology to boost your 3U system's performance and security.

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Learn More

VPX3-131 Freescale Power Architecture SBC datasheet

VPX3-133 Freescale Power Architecture SBC datasheet

White paper: Trusted Architecture - Data Protection with the QorIQ™ Platform Trust Architecture

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Freescale.com: The T2080 processor

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