

CHAMP-WB-DRFM

(VPX6-474-A04T000)

Xilinx® Virtex®-7 6U OpenVPX™
Card with Tektronix 12 GS/s
ADC/DAC Module



Applications

- ◆ Digital RF Memory (DRFM)
- ◆ Electronic Warfare (EW)
- ◆ Electronic Counter Measures (ECM)
- ◆ Wide-band, Low Latency, Sense & Response Applications

Benefits

- ◆ Large Virtex-7 FPGA tightly coupled with 12 GS/s ADC/DAC module
- ◆ Maximum I/O bandwidth
- ◆ Low Latency
- ◆ Large/Fast Memory Banks (2 64-bit DDR3L banks) 8 GB Total
- ◆ Standards based – OpenVPX™ 6U form factor

The CHAMP-WB is the first entry in Curtiss-Wright Controls Defense Solutions'

family of user-programmable Virtex®-7 FPGA-based computing products, designed to meet the needs of challenging embedded high-performance digital signal and image processing applications. The CHAMP-WB is targeted specifically at wide-band, low latency applications that require large FPGA processing, wide input/output requirements, with minimal latency. When combined with the TADF-4300 module, featuring 12 GS/s 8-bit ADC technology and 12 GS/s 10-bit DAC technology from Tektronix, an extremely high performance wide-band DRFM system can be created. The combined card-set is called the CHAMP-WB-DRFM.

The CHAMP-WB-DRFM couples the dense processing resources of a single large Xilinx Virtex-7 FPGA with a high-bandwidth 12 GS/s 8-bit ADC and 12 GS/s 10-bit DAC module in a commercial grade or rugged 6U OpenVPX™ (VITA 65) form factor module. The ADC device can also operate in a dual-channel mode, up to 6 GS/s. The CHAMP-WB-DRFM complements this processing capability with a data plane directly connected to the FPGA with support for Gen2 Serial RapidIO® (SRIO). Alternate fabrics can also be supported with different FPGA cores. A Gen3 PCI Express® (PCIe) switch connected to the Expansion Plane provides a way for a single host card, such as the VPX6-1957 or CHAMP-AV8, to control multiple CHAMP-WB-DRFM card sets without utilizing data-plane bandwidth. Two 64-bit 4GB DDR3L memory banks provide 8 GB of on-card data capture or pattern generation capability. An auxiliary x4 SERDES link and 16 LVDS pairs provide additional I/O capability.

The 12 GS/s ADC device goes through a pair of DEMUX devices presenting a 128 LVDS pair interface to the Virtex-7 FPGA. In parallel, a separate 160 LVDS pair interface connects the FPGA to the DAC device. A 100 MHz reference clock is generated on card or can be supplied by the back plane to both the ADC and DAC device. The clock is locally filtered to generate a clean sample clock

Learn More

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Sales Email: defensesales@curtisswright.com

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on the mezzanine for both the ADC and DAC device. The sampling clock can be adjusted with KHz resolution. In addition the base card supplies the primary power to the ADC/DAC module. The FPGA utilizes an I2C and SPI interface to the ADC/DAC module, to configure the module, calibrate the ADC/DAC devices and retrieve status.

This combination of enormous processing density and I/O bandwidth and flexibility make the CHAMP-WB-DRFM an ideal choice for many commercial or rugged embedded applications including electronic warfare, signal intelligence, ground penetrating radar and electronic countermeasures platforms.

Features

- ◆ OpenVPX™ (VITA 65) profile MOD6-PER-4F-10.3.1-x; MOD6-PER-1Q-10.3.5-2, VPX REDI (VITA 48 option)
- ◆ Single user-programmable Xilinx Virtex-7 FPGAs (X690T or X980T), with:
 - 8 GB DDR3L SDRAM in two banks
 - Four 4-lane serial data plane links to the backplane (support up to 10.3 Gbps data rates)
 - Gen2 SRIO or alternate fabrics can be supported with different FPGA cores
 - One 4-lane Gen3 PCIe connection to a Gen3 PCIe switch
 - 16 LVDS pairs to the backplane
- ◆ Populated with 12 GS/s (or dual 6 GS/s) 8-bit ADC and 12 GS/s DAC module
- ◆ Onboard PCIe Gen3 switch
 - Two 8-lane expansion plane fabric ports to the backplane with configurable NTB support
- ◆ Thermal sensors for monitoring board temperatures
- ◆ Sensors for monitoring board power consumption
- ◆ Support for ChipScope™ Pro and JTAG
- ◆ Backplane clock/sync paths to mezzanine sites

- ◆ Onboard programmable sample clock
- ◆ Onboard calibration
- ◆ Back plane Reference clock
- ◆ FXTools BSP and FPGA design kit with highly-optimized IP Blocks, development environment, reference designs, scriptable simulation test benches and software libraries VxWorks® and Linux® variants available
- ◆ VITA 48 1" pitch format
- ◆ Includes FPGA IP and software for data capture/generation, calibration and status collecting for ADC/DAC module
- ◆ Balun options for converting differential I/O to single ended
- ◆ Ruggedization levels
 - Air-cooled Level 0 (0 to +50°C)
 - Conduction-cooled Level 100 (-40 to +71°C)
- ◆ Path to variant with Processor (contact factory)
- ◆ For more information about the CHAMP-WB-DRFM please refer to the datasheet for the CHAMP-WB-DRFM

CHAMP-WB-DRFM Block Diagram

