Power Spikes Isolation to avoid corruption within sensitive ICs

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Introduction of spikes in systems during insertion of power supply jacks is observed in a majority of designs. These spikes are mainly caused due to:

- A very high frequency de-bounce on the power supply jack during insertion
- Equalization of ground between power adapter and battery-powered system

In most cases, the ICs on the board don't respond to such events. This is because they are either not yet powered by the board's main supply or they don't have sensitive electronics inside to react to it (in case of battery-powered systems).

Some of the electronic circuits that are generally affected are,

- Circuits which monitor the power line for variation, to detect tamper
- Circuits constructed for secure transaction authorization needs, such as tamper detection capabilities.

The following case study explains the way we went about resolving a power spike issue that is not common. As you will observe, the nature of the power spike in itself and the complexity of the design made the job tougher. The case study highlights the step-by-step method we followed to isolate and resolve the issue and our learning through this process.

Case study: Corruption within ASIC designed for tamper detection

We came across a situation where an ASIC chip for generating a secure code and storing it in a battery-backed RAM, was sensitive to these spikes. In fact, the function of the ASIC in the design was tamper detection, and spike was one of the kinds of tamper being detected. It was a catch-22 situation for us. The built-in tamper detection circuit was designed to detect excursions on its RAM supply and automatically erase the sensitive data to protect unauthorized data access. During the insertion/removal of power jack to the boards, the battery-backed RAM inside the on-board ASIC was getting corrupted as this was read as a tamper.

The system had two power sources: a Li-Ion battery and a 5V DC input through a standard wall power adapter.

The characteristic of the spike were as follows,

- It was in the GHz frequency range
- It had peak-to-peak amplitude of around 25V
- It appeared on all the signals on the board
- It occurred at the moment of contact of the power adapter to the board power jack
- It had both positive and negative swing.

Figure 1 shows a snapshot of the spike.

Figure 1: Snapshot of the spike

What made the job tougher was that,

- The spike caused ground bounce, which induced the spike in-turn to appear on all the signal lines throughout the board
- Due to the high frequency of the spike, it would jump layers on the PCB
- Use of decoupling capacitors that were placed very close to the battery, ferrite beads or FET switches (and any solid state isolation device) on the input power and ground lines were not a solution mainly because of the high frequency and energy of the spike
- If either supply or ground was isolated on the board, the spike would enter the board through capacitors at the input
- It had both positive and negative swing. Had the swing been towards a single direction, it would have been easier to address the issue.

Power supply load or power jack insertions de-bounce

Initially we approached the problem with a simplistic view and changed the power adapter suspecting that the adapter was not able to source enough power into the unit. We tried powering the unit using a battery as this is considered more regulated. We also loaded the adapter using a resistor assuming that if there was a steady flow of current, the power jack insertion will not introduce a sudden load to the power adapter and upset the DC/DC functionality inside the adapter.

Believing that the power adapter was not able to source enough power to the electronics on the board, we also put in Mega Ohm resistors in the path of power. The presence of Mega ohm resistor steeply decreases the current; thereby applying a minimal load on the adapter. Though the board doesn't power ON in this setup, the purpose of this experiment was to determine if the spike was caused by loading the adapter or due to the

mechanical insertion of the power jack. We observed that the power spike reduced by 5V in amplitude but this was not sufficient spike reduction.

Figure 2 shows a snap of the reduced spike.

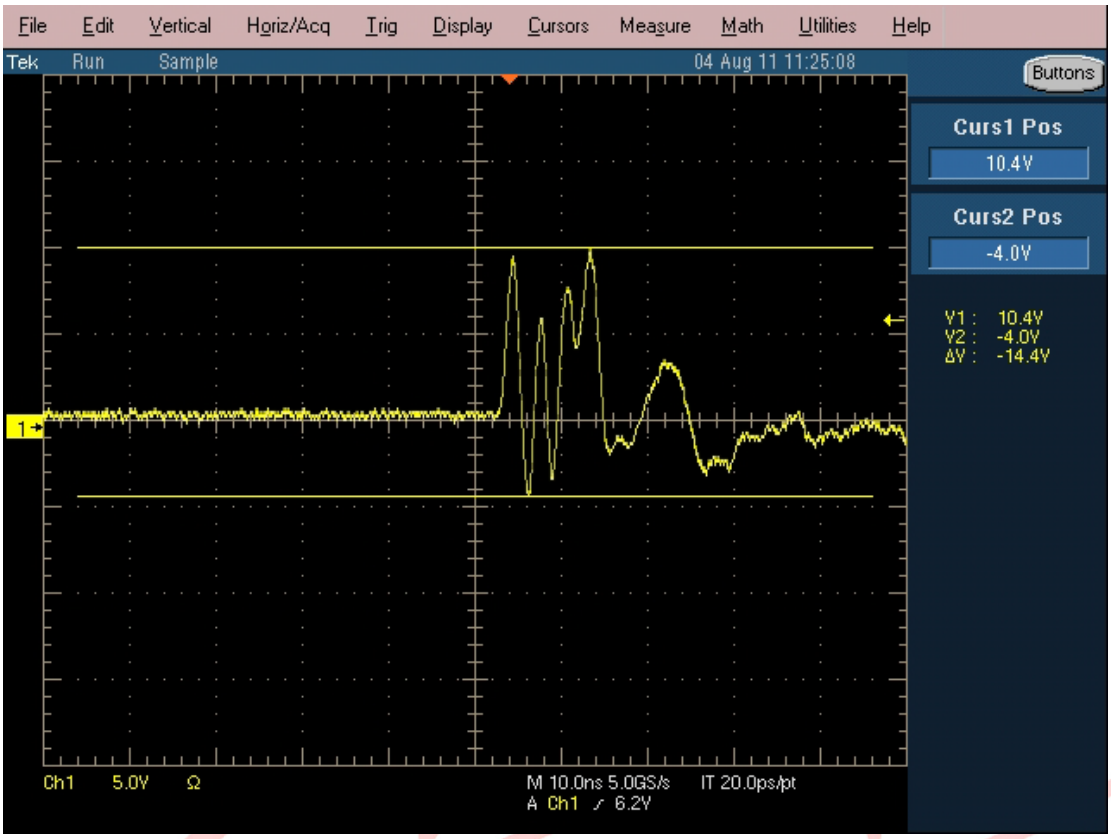

Figure 2: Snapshot of the reduced spike

As a next step to using the Mega Ohm resistor, we placed an NTC resistor in the power path to offer high resistance when the power was applied and slowly reduced the resistance to allow normal current flow. This only reduced the amplitude of the power spike by 5V.

Doing all these experiments made one thing clear; that this was not a power supply load issue. This was power jack insertions de-bounce. We tried changing the power jack but this did not help. We also tried using a slide switch assuming it would reduce the mechanical insertion issues; but this too did not remove the spikes.

Filtering out the spike

Having realized that the issue was due to the mechanical insertion, we wanted to filter out the noise from the power lines. To do this, we used the most frequently used filter, the LC filter, to block the noise. This too failed and we realized that the noise was not only on the power lines but on the ground layer as well.

Once we identified that the spike was occurring on both power and ground planes, we required a differential logic for the spike from both planes to compensate each other. We used a common mode choke across the power and ground lines. Since the two inductors are mutually coupled, we expected that the spike on one line would be induced on the other line as well, thus maintaining the same difference between power and ground in the output. This somehow did not work.

Slow starting the power

When the common mode choke experiment failed, we tried slow-starting the power to the unit similar to the ones we find in DC switchers, where a timing circuit can configure the time lag between the input power and stable output power. We put in FET switches on both the power and ground entry points, with a timing circuit to switch on power supply with a time lag, so that the spike due to the insertion of the power jack occurs but does not pass on to the electronics on board. This failed as the power spikes jumped the barrier junctions of the reverse protection diodes.

We followed this by placing reverse biased diodes in the path of power and ground lines assuming that diodes placed in the opposite direction of current flow would not allow the spikes to enter the electronics on board. This too failed as the spikes jumped these barriers as well.

Bypassing the power spike to ground

Next, we placed micro Farad range capacitors expecting them to store a lot of charge and aid in slowing the power on rise time by offering this capacitance to the power adapter. This also did not work as the capacitors did not react fast enough. Pico Farad range capacitors did not help either as they could not store enough charge to compensate for the spike. As a next step, we removed all the capacitors that were visible to the power adapter during insertion, given that capacitor appears as short at the moment of application of a step voltage. This momentary short might have caused power adapter to over correct its output because of high current flow and cause spike. All these did not help.

We also tried using TVS diodes but these are designed for high voltages but lower frequency of operation and they just did not react to the high frequency spike.

Transformer Based Isolation

At this point, we had to find a kind of isolation that was complete. This is when we thought about transformer based isolation. An isolation transformer provides complete isolation from primary to secondary both on the power and ground. The nature of transformer operation required the input to be varying. But, for handheld equipment, providing AC directly is not an option for want of space for the high power components. So, isolation transformers have to be used at DC levels. This solution uses a DC switcher to pulse the DC into a pulse transformer, which operates without hysteresis effects. The output was filtered using a high value capacitor. The power spike was isolated from the electronics by this kind of isolation.

Now to prevent the spike from appearing on all ASIC supplies, the ASIC section and related components had to be isolated from the remaining part of the board. To prove this concept, a test board was fabricated. This test board contained the ASIC, RAM backup battery and related components for ASIC to function. All the signals going from the processor to ASIC section were wired from the main board (existing design which had ASIC vulnerable to spikes). The ASIC section on the main board was disconnected from the processor.

The test board would draw both power and interface signals from the main board, which pass through isolators. The test board contained a DC-DC isolator to isolate both power and ground from the main board. Interface signals running from the main board to the test board pass through interface-specific isolators such as USB isolator and I2C isolators. All these isolators had separate power and ground pins for non-isolated (main board) and isolated (ASIC section of test board) section. Thus there was no direct connection between the isolated and non-isolated power and ground layers. The ASIC section was completely isolated from the main board.

During testing, it was observed that there were no spikes at the ASIC side of the isolators even though spikes were present on the other side (main board side). There was no path for the spike to reach ASIC section because only the isolators are present in between the ASIC section and the main board.

The block diagram in Figure 3 provides a logical representation of the isolation.

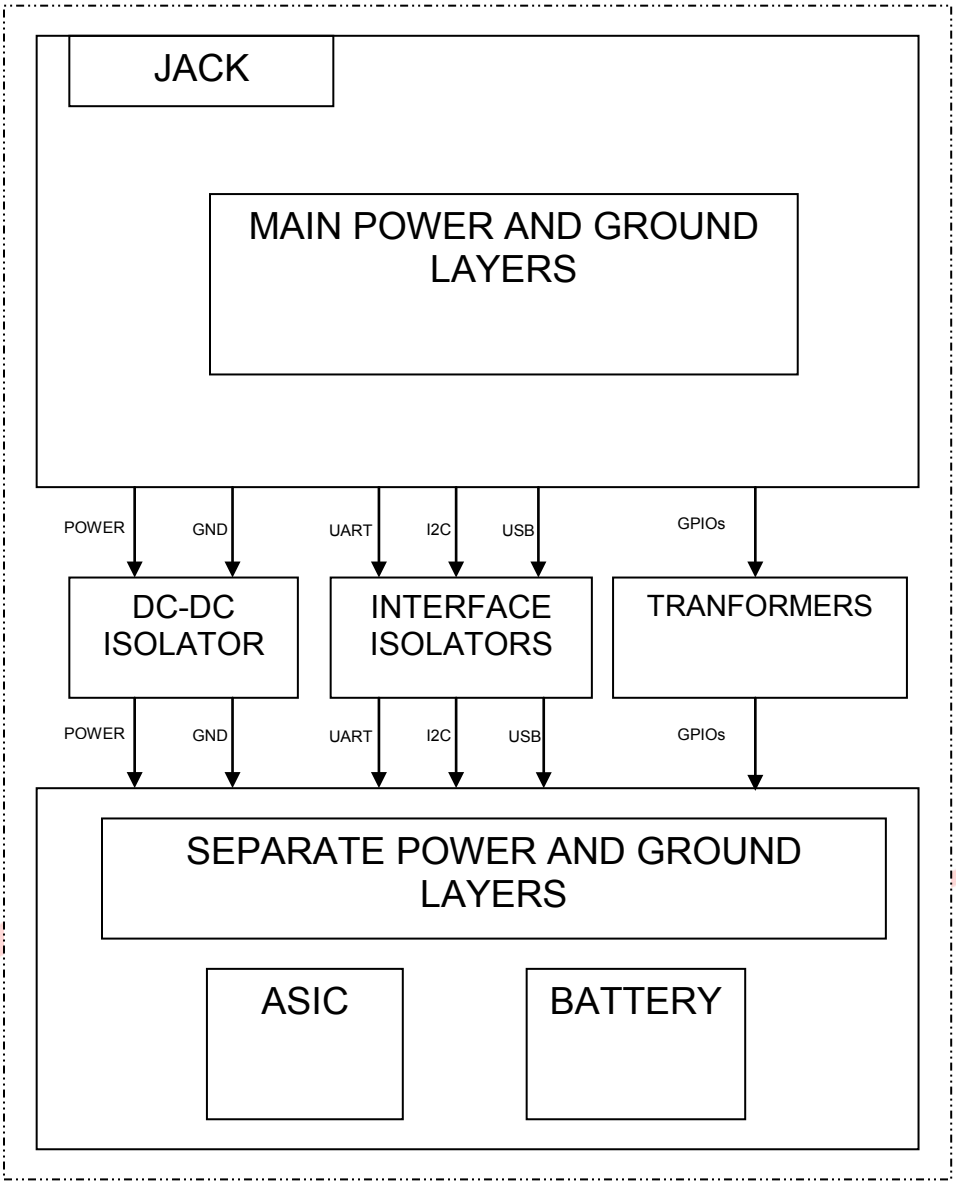

Figure 3: Block diagram showing logical representation of an isolation

Below are the schemes for the ground plane (Figure 4) and power plane split (Figure 5) that was required to realize the isolation on the same PCB.

Figure 4: Ground plane

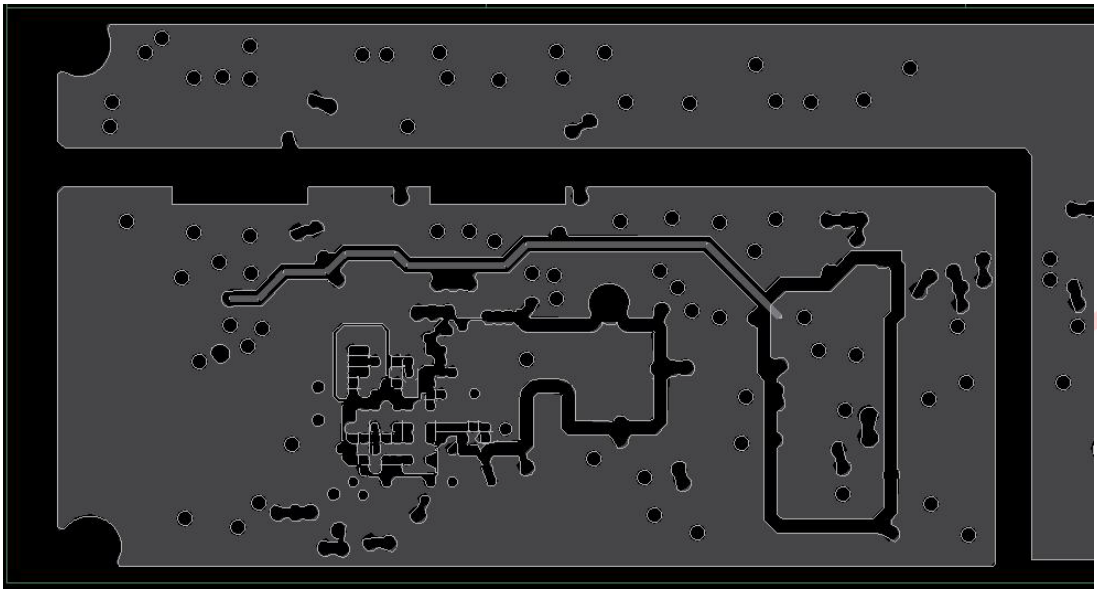

Figure 5: Power plane split

This kind of solution comes with a few constraints:

- High power rated transformers are needed, if isolation is designed right at the power input. This can be mitigated by using more isolation transformers on individual power rails, but again these are bulky components and will cause real estate issues on the board.
- All signal and power lines have to be isolated, if isolation is designed only for a section, but this needs smaller transformers.
- This solution is difficult to incorporate in a mobile environment. Advances in manufacturing technology will help here.

Why did isolation work?

Even though transformers respond only to variations in the input voltage, which in our case is caused by the spike, there is a certain cut-off frequency. Since we have used a low frequency power transformer with cut-off frequency in the range of hundreds of KHz, this GHz noise has no path for getting into the isolated circuit.

Advantages

Isolation, by definition, offers protection against high voltage induction and provides noise immunity. Selecting a transformer for the required application involves identifying the proper cut-off frequency and its harmonics.

Conclusion

When a sensitive IC is used in a design, isolation is very important. This should be achieved for both the interface signals using electronic components and ground by constructing the right plane split in the PCB. The power spikes are very high frequency signals and therefore, behave more like RF signals and jump over commonly used electronic barriers like filters, diodes and switches. If the power spike disturbs ground equalization the spike is observed everywhere. Complete isolation of the sensitive electronics in such cases is a good solution, but this comes at a cost (components, real-estate etc.) and the designer needs to make a balanced decision.

About the Authors:
Avinash Babu is a Sr. Architect with Mistral Solutions and has been instrumental is designing CE products like handheld devices, network video recorders, wireless cameras, rapid product prototyping modules and multimedia platforms based on ARM and PowerPC architecture.

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