High Speed Digital Design

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"**HIGH SPEED**" – These are two words that are bound to catch the attention of everyone in this generation. The need for speed is increasingly becoming a necessity in all applications of life rather than a luxury.

In today's modern world, we expect all our day-to-day tasks to be completed in no time. We wake up and turn on the shower to get hot water, grab a snack from fast food joints, and commute using high speed jets, trains, cars etc., while using smartphones with high speed bandwidth and so on.

To ensure convenience in our daily activities, there are engineers around the globe constantly innovating on solutions for High-speed Digital Designs.

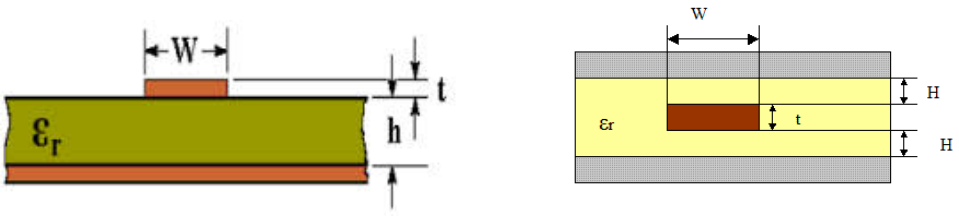
What is High Speed in Digital design?

When I first joined the industry 15 years ago, a 100 MHz to 200MHz speed was considered a high speed design. This was the core operating speed of SoCs and thus the peripherals were much slower. At that point of time, the rise and fall time of signals were not given much importance.

Today we are designing high-speed boards which are capable of operating at speeds of up to 10G at very low voltage levels. Future designs will or might be capable of operating at a few 100G. To meet this increasing demand, where the frequency of operation has to change with respect to time, new techniques are required. In this article, I'll be touching upon some of these techniques.

PCB Components affecting High-speed Digital designs

An ideal design is that which has no losses in the transmission lines. The transmission line or media can be a trace in PCB design or a cable. When creating a trace in PCB design, the designer needs to consider a proper reference for the transmission line. There needs to be a solid ground plane as a return path. The transmission line on PCB can be a Micro strip or a strip line.



Microstrip **Stripline**

Fig. 1: Parameters for defining trace width
Image Source: Circuits Online

Trace Widths

The width of the trace (W) is defined by various parameters as shown in the diagram. To enable engineers to perform this calculation, there are tools or calculators which help in designing. In general, wider traces are better, but to maintain a 50 ohm impedance for single end and a 100 ohm for differential pairs, along with a constraint on Board space and layers, we will need to trade off on the wider trace widths. Fig. 2 is a snapshot of the commonly used tool for trace width calculation.

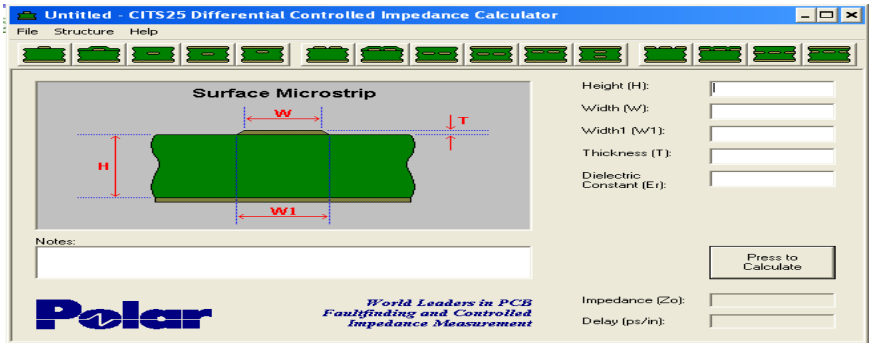


Fig. 2: **Tool from Polar for trace width calculation**

Dielectric Material

It is very important to define the dielectric materials in the PCB design, especially at high frequencies as at such frequencies the dielectric loss is dominant.
The relative permittivity (εr) of the dielectric material defines the degree to which an electromagnetic wave is slowed down as it travels through the insulating material. A material with lower value of (εr) is almost always better or preferred for being used in High-speed Digital designs. As lower the (εr) of the material, it will tend to have a lower loss tangent.

The (εr) in general is measured at 1.0 MHz for FR4 material as standard. Some of the materials with their (εr) along with loss tangent are mentioned below:

Material	(εr) at 1.0 MHz	Loss tangent
FR4	3.9 to 4.6	0.02 to 0.03
FR408	3.4 to 4.1	0.01 to 0.015
Nelco	3.2 to 3.7 at 1 GHz	0.005 to 0.01
Rogers	3.4 at 10 GHz	0.002

Table 1: **Dielectric Materials for use in High-speed digital design**

Vias

Vias are usually not considered in most designs, but for High-speed Digital Designs, Vias are given utmost importance and have to be treated as a small trace. Generally, using Vias is avoided, but in case a Via is used, we will have to think of options to reduce the short trace length. So how exactly do we address this?

Vias needs to be Backdrilled.

Fig.3 gives an idea of connectivity with a back drilled Via.

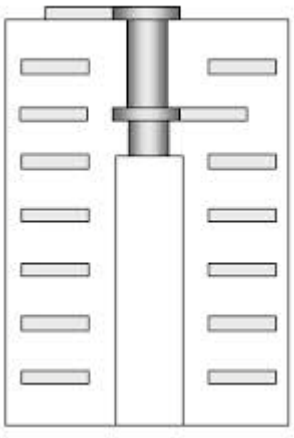


Fig. 3: **Back drilled Via**
Image Source: Blog - Lamsim Enterprises

The Return Path or reference for the Vias is also an important consideration and high-speed Digital design boards are provided with stitched Vias to address this. These stitched Vias need to be provided all throughout the board by connecting to Ground planes which provides a good return path for the signal as compared to the reference plane.

There are several other aspects to look in to when we talk about High Speed Digital Designs.

Pre Layout & Post Layout Simulation (Signal Integrity) –

What is the Difference?

Pre-Layout is done prior to the board layout on the design while Post-Layout is done after completing the board layout. These simulation results and the analysis of the simulation results form the key to the High speed digital board designs.

The simulations are carried out to ensure that the design is feasible and the end result, a working PCB can be achieved with minimal design changes during the test phase of the board.

Pre-Layout simulations provide data for deriving a board concept and constraints. Post layout gives the result / confirmation of applying the board concept and constraints to ensure that the signal / transmission line is as per the given requirement.

It is important to perform these simulations and Mistral has been actively carrying out these activities especially on designs intended for having High Speed Digital interfaces.

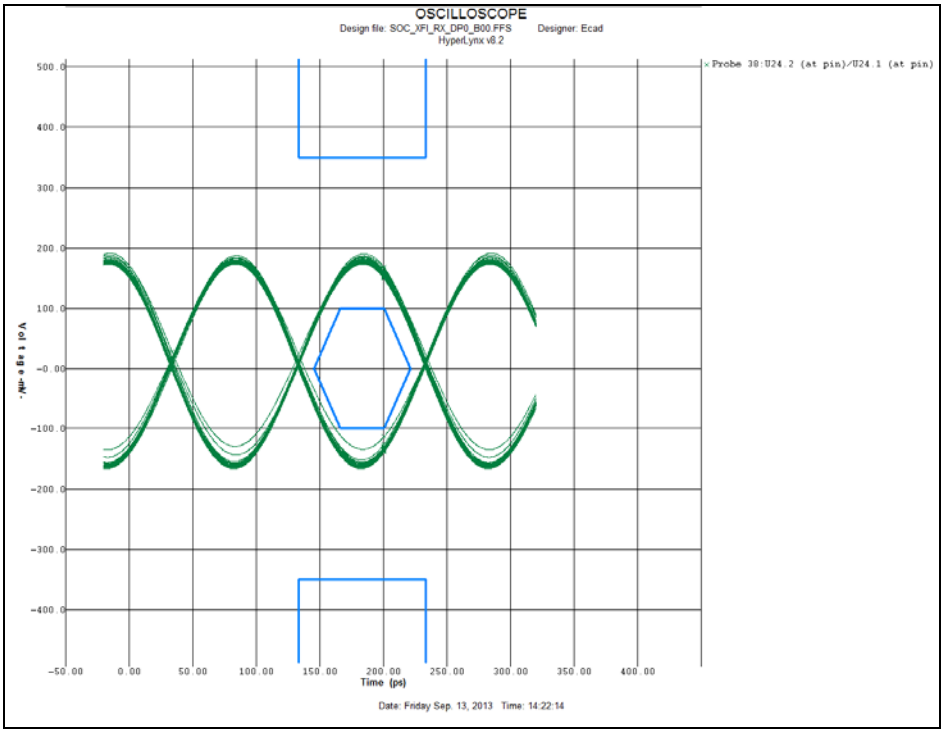


Fig. 4: Post simulation result for 10GHz on RTM BOC

Decoupling Techniques (Power supply Bypass capacitors for High-speed Active Components) –

Let us start by looking at decoupling capacitors right from the power source of the board.

Appropriate decoupling capacitors needs to be provided at source. Selection of the decoupling capacitors is very important, as improper values in decoupling capacitors could increase the noise floor in the board. Also due to technology advancements, we aim for lower voltage levels at higher frequency due to which digital signals may not be detected appropriately.

When power distribution takes place (Digital and PLL), we need to add appropriate ferrite beads for separation along with decoupling capacitors. Sufficient decoupling capacitors have to be provided for all the active components near the power supply pins. We also have to connect the Capacitors to Power and Ground planes with as short traces as possible.

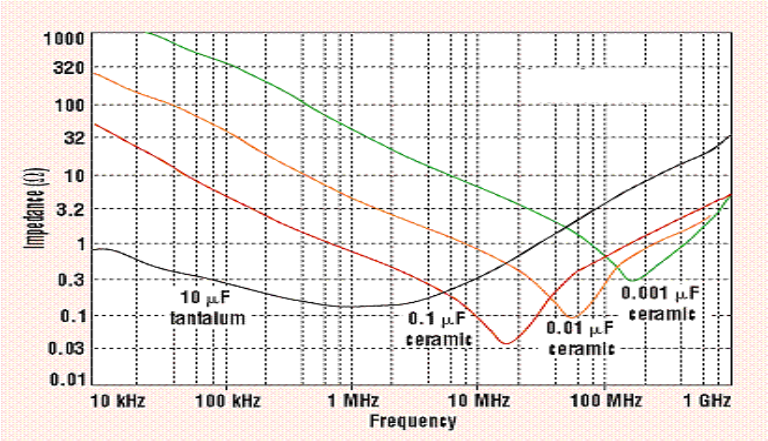


Fig. 5: Frequency response curve for decoupling selection

High-Speed digital Boards designed by Mistral

Below are two boards (RTM Breakout card and AMC Break out card) designed by Mistral as plug in boards for the keystone family EVM's. These Break-out cards can be used to build application boards involving high speed design interfaces.

The typical High speed interfaces on these boards are listed as below:

- PCIe
- AIL
- SGMII and
- SATA

RTM BOC

AMC BOC

Fig. 6: RTM BOC and AMC BOC

Apart from theory, here are a few points or details that an Engineer has to understand while taking up a High-speed Digital Design:

- Preferably use only surface mount components
- Know the maximum frequency of operation on board
- Define a proper stack up for PCB
- Perform a layout analysis for placement and routing, share the data with the layout engineer for better output
- Analyze the results of pre-layout simulation and work on getting better results
- Keep the traces as short as possible
- Avoid Vias as much as possible
- Maintain the skew and spacing as per guidelines
- Add Ground plane on the space available in routing layers, stitch ground Vias to the Ground planes
- Keep high speed interfaces away from other signals by giving sufficient spacing 3 to 4x
- Keep the high speed traces as straight as possible and avoid unnecessary bends in signal (90 Degree bend is to be 100% avoided)
- Add Guarding (Ground signal around the High speed Signal) to signals like high speed clock etc. wherever possible

*Reference: "**A Handbook of Black Magic by Howard Wesley Johnson**"*