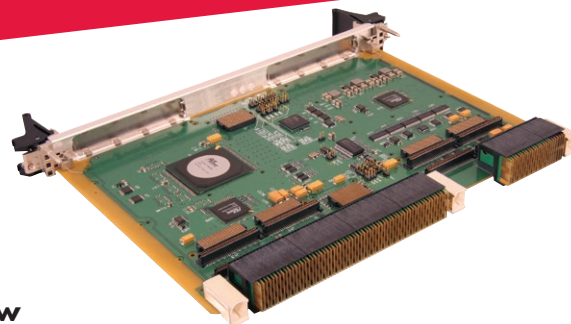




# VPX6-218

## 6U OpenVPX™ XMC Carrier Card



### Features

- ◆ The backplane fabric follows VITA 65 P2 expansion plane providing a Quad Fat Pipe (QFP) to P2
  - VITA 65 peripheral module profiles
    - MOD6-PER-1Q-12.3.5-1
    - MOD6-PER-1Q-12.3.5-2
- ◆ Two XMC sites:
  - 8-lane PCI Express® (PCIe) Gen2 interface
  - VITA 46.9 signal mapping:
    - P3w1-P64s+P4w1-X12d+X8d+X24s
    - P5w1-P64s+P6w1-X12d+X8d+X24s
  - 25W mezzanine support

### Overview

The VPX6-218 XMC carrier card provides great flexibility to system integrators needing to expand their OpenVPX-based systems' I/O complement via standard XMC modules. A PCIe Gen2 connection over the VPX™ backplane allows host processors to access a high-performance, low latency native PCIe interface to the VPX6-218 carrier card.

The XMC sites of the VPX6-218 provide flexibility in the range of modules supported including the latest generation high-performance XMC utilizing 8-lane PCIe Gen2. To a host processor, XMC modules on the VPX6-218 appear as if they were on the host processor.



### Learn More

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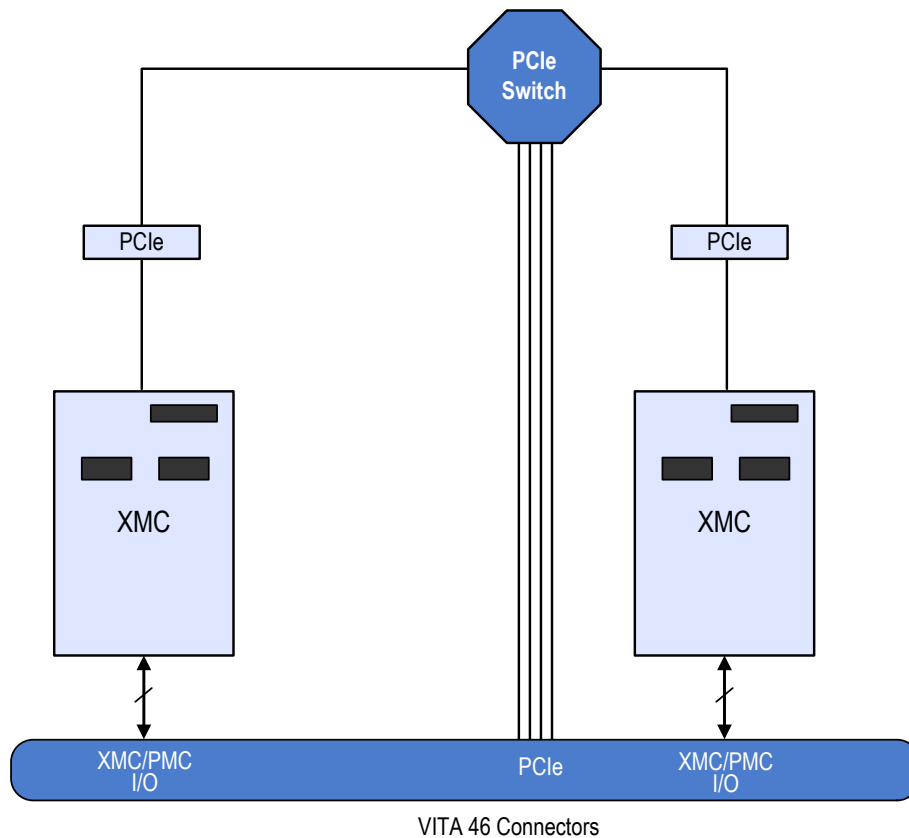
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Figure 1: VPX6-218 Block Diagram



### Backplane Fabric Ports

The VPX6-218 connects to other cards via four, 4-lane PCIe ports thru the VITA 46 P2 connector. All PCIe ports go through a PCIe switch.

The backplane can be selected to function as either four, 4-lane PCIe ports or as two 8-lane upstream ports. The selection of lane width is via on-board jumpers, as is the choice of which backplane PCIe port is the upstream port.

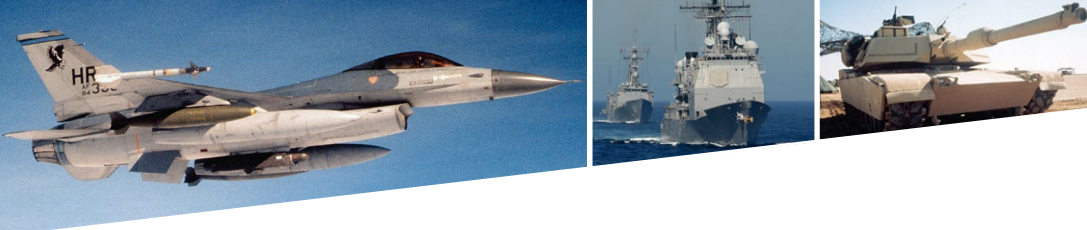
Note that there can only be one active upstream port. The VPX6-218 also had a BOOT configuration EPROM for the PCIe switch which can be written to through the I2C interface.

### XMC Sites

The VPX6-218 is equipped with two mezzanine sites, each capable of supporting VITA 42.3 XMC modules. The VPX6-218 takes full advantage of the VPX standard by providing 64 signals (32 pairs) of Jn4 I/O and 40 signals (20 pairs) of differential Jn6 I/O from each of its mezzanine sites to the backplane connectors. The I/O is mapped according to the VITA 46.9 specification which provides for controlled impedance, matched length differential pairs. There are also 24 single-ended signals from Jn6.

Both XMC sites utilize up to an 8-lane PCIe Gen2 host interface on the Jn5 connector.

On conduction-cooled cards, the XMC sites adhere to the VITA 20-2001 (R2005) conduction-cooled PCI mezzanine card standard specifications. To optimize the thermal transfer from XMC modules to the base card, the standard VPX6-218 thermal frame incorporates both the primary and secondary thermal interfaces as defined by VITA 20-2001.



**Table 1: XMC Site Specifications**

Function	Site 1	Site 2
Location	Top center of card	Bottom center of card
PCI Interface	None	None
PCIe Interface	Up to 8-lane per VITA 42.3 4 Gb/s peak simultaneous transmit and receive	Up to 8-lane per VITA 42.3 4 Gb/s peak simultaneous transmit and receive
Jn4 I/O	64 signals (32 pairs) to VITA 46 P3 per VITA 46.9, rule 5-5, pattern P3w1-P64s	64 signals (32 pairs) to VITA 46 P5 per VITA 46.9 rule 5-5, pattern P5w1-P64s
Jn6 I/O	40 signals (20 pairs) to VITA 46 P4 per VITA 46.9, rule 5-5, pattern P4w1-X12d+X8d+X24s	40 signals (20 pairs) to VITA 46 P6 per VITA 46.9, rule 5-5, pattern P6W1-X12d+X8d+X24s
Differential Routing	100 Ohm differential, 50 Ohm nominal for both Jn4 and Jn6 I/O signals	
3.3V Power	Provided from on-board PSU, 13W maximum to each site. The 3.3V is sequenced with the main board power.	
5.0V Power	None	
12V	Power for XMCs is selectable and provided by a 12V backplane. Max power is 20W.	

The VPX6-218 is capable of hosting processor XMCs in monarch mode as described in the VITA 32-2003 draft standard.

The table above, XMC Site Specifications, provides details on the capabilities of both mezzanine sites.

### Status Indicators and Controls

The VPX6-218 supports two front panel indicator LEDs. A Red Fail LED is provided that will be on if any of the on-board power supplies are out of specification; the default state is OFF. A Green Status LED is provided that is on when the VPX6-218 is out of reset.

Each PCIe port for the backplane fabric ports and on-board PCIe ports has an indicator LED that, when lit, indicates the port has been trained and is operational.

### I2C

The VPX6-218 has the ability to connect to a I2C interface from the backplane P0 connector to program the PCIe switch EPROM.

### Specifications

The tables below show the power, dimensions and weight characteristics of the card.

**Table 2: Power Requirements**

3.3V <sub>AUX</sub>	500 mA
5V (VS3)	Not used
12V (VS1/VS2)	800 mA
12V <sub>AUX</sub>	Not used
-12V <sub>AUX</sub>	Not used

**Table 3: Dimensions and Weight**

Option	Dimensions	Weight (grams)
Conduction-cooled Level 200	Per VITA 46 draft 0.8" pitch	<800 g

\*Refer to Ruggedization Guidelines fact sheet for more information.

### Ruggedization Levels

Conduction-cooled cards are available in Level 200. See the Curtiss-Wright Ruggedization Guidelines fact sheet for more information.

Circuit card assembly is designed and manufactured to Class 3 standards of IPCA-610C, Acceptability of Electronic Assemblies. Standard conformal coating is acrylic.



## **Warranty**

This product has a one year warranty.

## **Contact Information**

To find your appropriate sales representative:

Website: [www.cwcdefense.com/sales](http://www.cwcdefense.com/sales)

Email: [ds@curtisswright.com](mailto:ds@curtisswright.com)

## **Technical Support**

For technical support:

Website: [www.cwcdefense.com/support](http://www.cwcdefense.com/support)

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