TECHNOLOGY WHITE PAPER

FMC to FMC+: Keeping Up with New FPGAs and Analog I/O

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DEFENSE SOLUTIONS

Read About

FPGA Mezzanine Cards (FMCs)

Analog I/O

JESD204B

VITA 57.4

FMC+

Introduction

Mezzanine cards are an effective and widely used way to add specialized functions to an embedded system. Because they attach to a base card or carrier card, rather than plugging directly into a backplane, mezzanine cards can be easily changed. For system designers that means both configuration flexibility and an easier path to tech upgrades.

Different mezzanine standards have different strengths and weaknesses because there are trade-offs between competing requirements for size, functionality, power and impact on their host - and the best standards have been adapted to technology and market requirements over the years to ensure they stay relevant. FPGA Mezzanine Cards (FMCs), under the banner of VITA 57, are exposed to technology change more than most mezzanines standards because they connect I/O devices directly to FPGAs rather than through industry standard busses such as PCI Express® (PCIe). FMCs exist to provide I/O to FPGAs – high bandwidth I/O to keep increasingly powerful FPGAs fed with data, so their processing operations proceed without waiting.

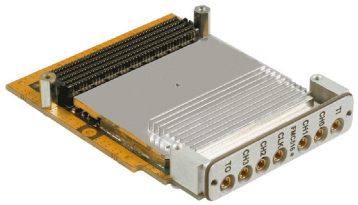

Figure 1: FMCs exist to keep FPGAs fed with I/O

FPGAs have got faster, especially with signaling speeds interfacing to I/O devices (usually analog I/O) and have also leapt forward in terms of I/O channel density, resolution and sample rates. The FMC standard has coped well and has become the open standard mezzanine of choice, but is it running out of capability? If it is, can it adapt and what is possible with the FMC format today and in the future?

The FMC standard defines a small format mezzanine, similar in width and height to XMCs or PMCs, but around half the length. This means FMCs have less component real-estate than many other open standard formats. However, FMCs don't need bus conversion, such as PCI-X, and have simplified power supply requirements which means that FMCs could actually have more I/O capacity than their XMC counter parts. Let's break this down.

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FMC Operating Characteristics

First, FMCs directly connect the I/O devices on the mezzanine to the host FPGA via a high speed, high density connector as if the device was on the host itself. This means little, if any, interface logic is required. Next, although the FMC defines a number of power supply requirements, its primary power is provided by the host. As part of the host/mezzanine power up sequence, the FMC is interrogated by the host as to what its power supply requirement is. As long as the host can provide the requested voltage, the FMC power up sequence will continue. This means the FMC power supply design is simplified, though for analog functions low noise regulation is recommended. In all, this means that the FMC often contain the I/O devices and nothing else other than EEPROMs with the information required by the power up interrogation. This makes FMCs very efficient in terms of I/O real-estate.

The FMC specification is a little unusual in that there is no requirement that connectivity to the FMC connector is complete. Some FMCs (or hosts) need only provide a subset of functionality, so the specification defines how this connectivity is provided by defining the order in which I/O pins on the FMC connector are built up. For example, if the host and FMC mezzanine have 60 connections, they are the same connections. This means the capability of both the host and mezzanine need to be checked to ensure sufficient connectivity is provided. The FMC specification allows for up to 160 (for HPC – high pin count) or 80 (for LPC – low pin count) "parallel" I/O signals and up to ten full duplex high speed serial connections (along with some clocks).

FMCs for Analog I/O

Although FMCs can be used for any function that you might want to connect to an FPGA, such as digital I/O, fiber-optic, control interfaces, memory or additional processing, it is analog I/O that is most common. It has not been lost on analog device vendors that the FMC format is a good standard for evaluation cards since the higher performance ADCs and DACs invariably use FPGAs to provide interfaces and front end processing. The willingness of major device manufacturers and FPGA vendors to implement the FMC format is good for early technology adopters and insures that the FMC standard will continue to be used, provided it can evolve.

The FMC specification affords a great deal of scope for fast, high resolution I/O, but there are still trade-offs – especially with high speed parts using parallel interfaces. Take, for example, Texas Instrument's ADC12D2000RF dual channel 2 GSPS 12-bit ADCs. These parts use a 1:4 multiplexed bus interface, so the bus speed is not too fast for FPGAs. The digital data interface alone requires 96 signals (48 LVDS pairs) for a device of this class so only one of these devices can be supported, even if there is sufficient space for more, because of the 160 signal limit. Lower resolution even at higher speeds, such as those with 8-bit data paths, may allow a second channel.

Similarly, slower devices require little if any multiplexing and fewer connections means smaller devices too. In this case, quad and octal analog I/O (or more) is possible for sub 1 Gsps analog I/O per channel. In reality though, even if there was more FMC connectivity available to support two of these ADCs, the pin count and package size means that fitting them both onto an FMC is not realistic. The additional requirements of the front end analog coupling of the baluns or amplifiers, clocking, etc. means that the amount of real-estate required probably crosses the limit of what is practical for high speed I/O channel density on the FMC format even if more connectivity could be provided through parallel interfaces. Faster, higher speed, higher resolution parts would strain this further as wider multiplexed interfaces would be required at a certain point in order to support the FPGA interface. Even with newer generations of FPGAs, effects such as skew become more difficult to deal with.

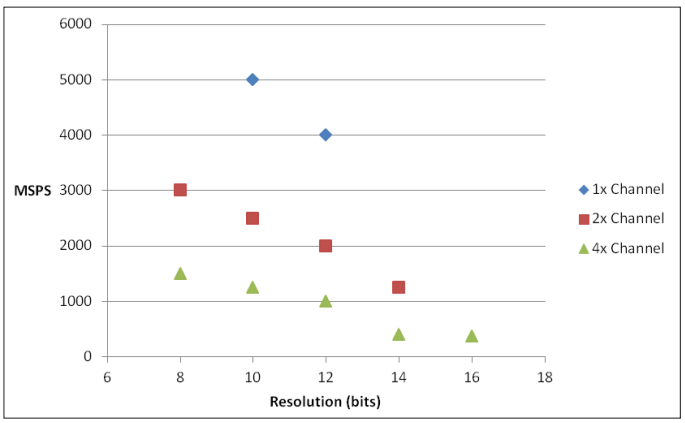

Figure 2: FMC-base ADC options

The FMC specification starts to run out of steam with analog interfaces delivering >8-bit of resolution at around 5 Gsps or 6 Gsps throughputs of >50 Gbps using parallel interfaces. From a market perspective, leading FMCs based on channel density, speed and resolution are in the 25 to 50 Gbps range. See the graph in Figure 2 for a snapshot of FMC-based ADCs, with sample rate/resolution/channel density (using information available from the internet). This functionality results from a trade-off between physical package sizes and available connectivity to the host FPGA.

In addition to the maximum 160 HPC connections, the FMC specification also provides for High-speed Serial (HSS) links with up to ten full duplex channels. These are useful for such functionality as fiber-optic I/O, Ethernet, emerging technologies such as Hybrid Memory Cube (HMC) memory and newer generation analog I/O devices using the JESD204B interface recently adopted by high speed devices. These HSS links are sometime used, for example, to connect an ADC leaving the parallel interface to drive a DAC should the number of parallel signals be insufficient to support both functions.

Enter JESD204B

Although the JESD204 standard, currently at revision 'B', has been around a while, it is relatively recently that it has gained wider market penetration and become the serial interface of choice for newer generations of multi-GSPS data converters. This wide adoption has been stoked by the telecommunications industry's thirst for ever smaller, lower power and lower cost devices. A dual channel 2 GSPS/12-bit ADC with a parallel interface, as mentioned earlier, requires 96 signals alone for the data interface. This directly impacts the package size, in this case a 292 pin package ~27 x 27mm square, though newer generation pin geometry could shrink this down to perhaps something less than 20 x 20mm.

A JESD204B connected equivalent can be provided in a 68 pin 10 x 10mm package – with reduced power. This is a dramatic reduction in package size and marries up well to evolving FPGAs which are providing ever more HSS links at higher and high speeds. Typical high speed ADCs and DACs using the JESD204B interface have between 1 and 8 HSS links operating at 3 to 12 Gbps interfaces, depending on the data throughput required based on speed, resolution and number of analog IO channels.

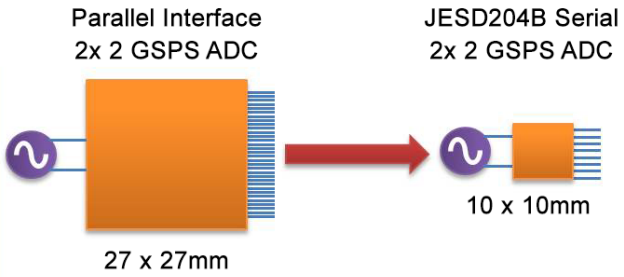

Figure 3: Package size reduction effect using JESD204B Interfaces

The FMC specification defines a relatively small mezzanine standard, but with the emergence of JESD204B devices there is room to fit more parts onto the available real-estate. The maximum of 10 HSS links defined by the FMC specification is a useful quantity. Even this limited number of HSS links provides another 80 Gbps+ of throughput, but using a fraction of the pins required for parallel IO.

The emergence of serially connected I/O devices, not just those using JESD204B, does have drawbacks for some applications such as EW (Electronic Warfare). This is because serial interfaces invariably introduce additional latency due to longer data pipelines within the I/O devices. For EW applications latency is the fundamental performance parameter, above speed or resolution. Although latency is likely to vary widely between serially connected devices, even within the JESD204B framework, new generations of devices will push data through the pipelines faster and faster, with some promising the ability to tune the depth of the pipeline.

Some standard ADC devices sampling at >1 Gsps today have sub 100ns latency, though to be properly embraced by the wider EW community this needs to be improved by an order of magnitude. Other applications can tolerate this latency, or do not care about it, including receiver only applications such as Radar Warning Receivers (RWR) or COMINT. For these applications there are large advantages to be gained by using a new generation of RF ADCs and DACs, a technology driven by the mass market telecommunications infrastructure.

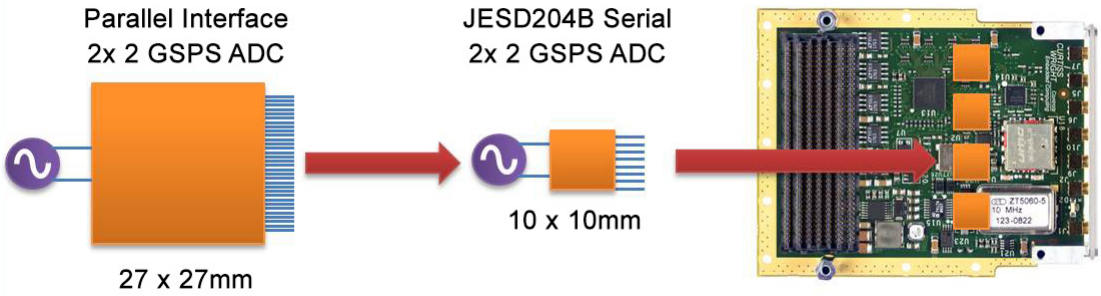

Figure 4: Effect of package shrink on FMC through JESD204B

JESD204B based devices do still have challenges in achieving the very accurate synchronization of high speed 1 to 10 Gsps+ devices, but new strategies are emerging. Some synchronization capabilities are now built into devices using vendor specific signaling, to support functions such as accurate direction finding (DF) and beamforming that are common to both defense and telecommunications applications.

An advantage provided by JESD204B, perhaps as a side effect, is the increased number of analog channels. To keep high speed ADCs and DACs from becoming impractically large, the number of I/O channels on each device has been limited. Now, with fewer IO pins required by JESD204B interfaces, devices are emerging that support more analog channels. Apart from gains made by a greater number of analog channels per square inch, having more channels on a device is better suited to interleaving and thus higher sample rate options through improved synchronization and channel matching.

Outside of the FPGA community, JESD204B is also starting to be adopted by newer DSP devices. However, because they deliver the type of performance that can deal with vast volumes of data, FPGAs are likely to remain the stronghold in exploiting the capabilities of wideband analog I/O devices.

The Evolution of the FMC Specification – FMC+

The FMC specification is evolving to take advantage of serially connected FPGAs and I/O devices. The size advantage of the smaller JESD204B devices means that more of them can be fitted on an FMC footprint. To take full advantage of the newer devices coming onto the market, FMCs need more serial connections.

An effort to define suitable FMC enhancements is now underway within the VITA 57.4 working group. The focus is on creating a specification with an increased number of HSS links operating at increased speed (along with additional clock I/O) under the preliminary “FMC+” name. FMC+ aims to provide full FMC backward compatibility by adding to the FMC connector’s outer columns for the additional signals and not changing any of the board profiles or mechanics.

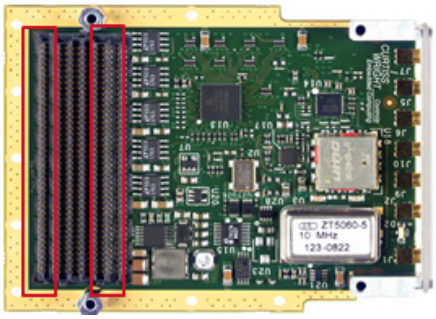

Figure 5: Additional connector rows for FMC+

The additional rows, because they will be part of an enhanced connector, will minimize any impact on available real-estate. The outline of FMC+ specification increases the maximum number of available HSS links from 10 to 24; there is an additional connector option outside the usual FMC physical envelope to 32 full duplex channels for host/FMC+ combinations that require yet more capability and connectivity. Through high speed characterization, the throughput per HSS link is increased to 28 Gbps in each direction, though host and FMC+ combinations will require careful design to achieve these speeds. This takes the maximum full duplex throughput to over 900 Gbps in each direction, if the parallel interface is included.

The increased throughput enabled by FMC+ can be applied to enable new devices with a range of capabilities. There are various trade-offs, such as mechanically how many devices can fit at on the mezzanine real estate, resolution and sampling bandwidth. Figure 6 shows the expansion of available options with FMC+.

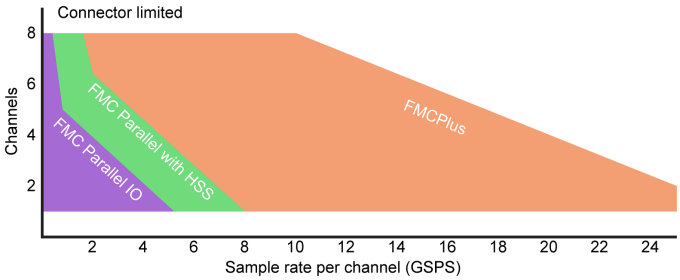

Figure 6: FMC vs FMC+ throughput capability

It should be noted that the FMC+/VITA 57.4 is being developed and could still change, but VITA recognizes the need for this specification enhancement and the need to release this in good time.

Next Generation ADCs & DACs

In the next few years, it is reasonable to expect high resolution ADCs and DACs to break through the 10 Gsps barrier to support wideband communications with direct RF samplings for L, S and even C-band frequencies. Below 10 Gsps, converters are emerging with 10, 12 or even 14-bit resolutions, with some supporting multiple channels. The majority of these devices will be using JESD204B (or a newer revision) signaling with 12 Gbps channels until a new generation cranks this speed even further, which is inevitable. These fast moving advances are fueled by the telecommunications industry, but the military community can take advantage of them to meet SWaP-C requirements – especially if there is mezzanine support such as FMC+ for fast prototypes and system flexibility.

Other Advantages and Uses of FMC+ Mezzanine Cards

Although FMC+, like FMC, is likely to be dominated by ADC, DAC and transceiver products, the increased HSS density provided by FPGA makes it useful for other functions. Two functions of note are fiber-optics and new memories.

As with JESD204B, there are requirements for higher speed and higher density fiber-optics, with those based on fiber-optic ribbon cables offering the smallest parts. Up to 24 of these new devices are viable in the FMC+ footprint; they may reflect where the higher speeds of FMC+ will be realized first. Bandwidths of 28 Gbps per fiber will take the throughputs quickly past 100 and 400G speeds on a single mezzanine. 100G optical throughput is emerging today on the current FMC format.

Another emerging function suitable for FMC+ is memory through the introduction of the HMC. HMC's small footprint, together with the good HSS connectivity, could mean that high capacity memory modules become available in the near future.

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Summary

A new generation of the FMC specification, adapting to new technology driven by serial connected devices, is being developed and gathering pace. The FMC standard, through its new incarnation, FMC+, is alive and kicking and being prepared for the next generation of high performance, FPGA driven applications. Watch this space.

Learn More

Analog I/O and Digital Receivers

FMC-516: Quad 250 MSPS 16-bit ADC FMC

FMC-518: Quad 500 MSPS 14-bit ADC FMC

FMC-520: Quad 550 MSPS/Dual 1 GSPS 16-bit DAC FMC

FMC-XCLK2: Multi-Channel Clock Generator

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