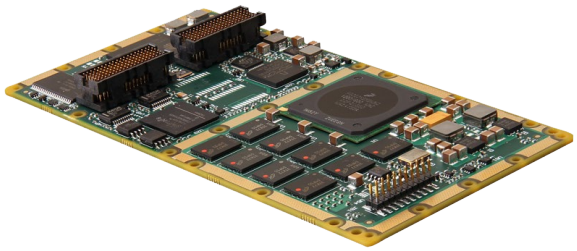
Data Sheet

XMC-109

Freescale™ Power Architecture® QorIQ™ P2020 Processor Mezzanine SBC



Features

- Freescale QorIQ P2020 up to 1.2 GHz
  - Two e500 processor cores
  - Each core has 64KB L1 cache
  - 512KB shared L2 cache with ECC
  - Single DDR3 memory controller with ECC
  - Two Gigabit Ethernet controllers
  - Single DUART
  - One I2C channel
  - One PCI Express® (PCIe) interface
  - Two 4 channel Integrated DMA controllers
- Up to 8GB DDR3 SDRAM with ECC in a single memory bank
- 256MB NOR flash with write protection
- Optional 8GB onboard NAND flash
- Permanent Alternate Boot Site (PABS) provides backup boot capability
- 512KB FRAM
- Two Gigabit Ethernet interfaces
  - configurable as 1000Base-X or 1000Base-T
- Two asynchronous EIA-232/422 serial ports
- 4 LVTTL discrete I/O signals
- Optional one SATA 2 port
- One USB 2.0 port
- Six general-purpose 32-bit timers in core functions FPGA
- Eight global timers organized as two groups of four in the P2020 Multi-core Programmable Interface Controller (MPIC)
- Two avionics-style watchdog timers
- Real Time Clock with +3.3VAUX switch over
- Two temperature sensors
- U-Boot with extensive diagnostics
- Wind River® VxWorks® 6.9.3 Workbench® 3.3 support
- Wind River Linux® 4.3
- Range of air- and conduction-cooled ruggedization levels are supported

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Overview

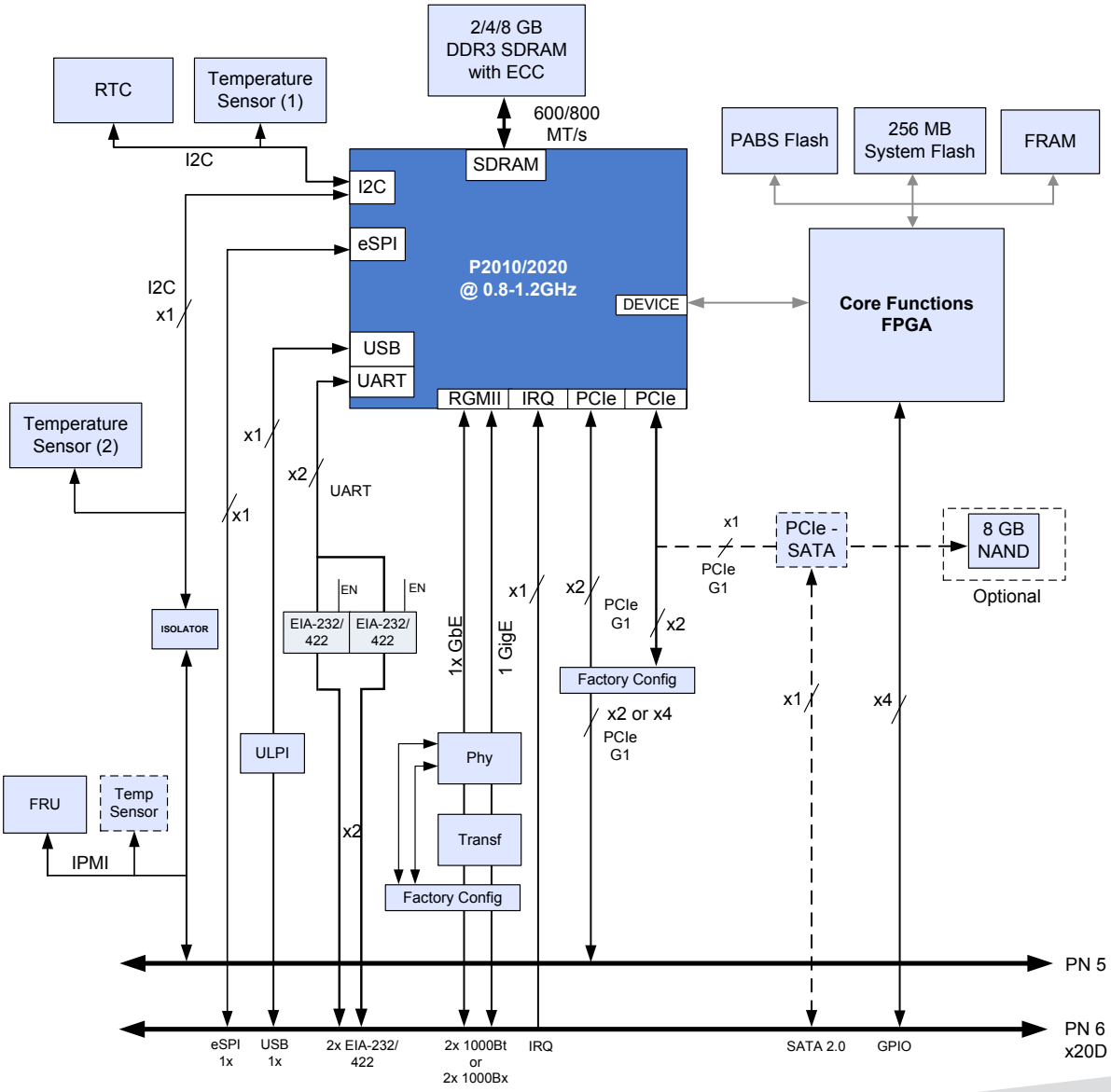
The XMC-109 is the next generation of XMC mezzanine single board computer (SBC) from Curtiss-Wright Defense Solutions. It is targeted for applications with moderate processing, low power and low cost requirements.

The XMC-109 is based on Freescale's QorIQ P2020 SOC multi-core processor. The XMC-109 provides high-performance processing, and a long list of features and I/O interfaces to satisfy the demanding requirements of embedded computing.

Available in a full range of environmental build grades, the XMC-109 is targeted to the control requirements for rugged embedded systems such as tactical aircraft, armored vehicles, harsh environment naval systems or industrial applications.

The XMC-109 occupies a single standard VITA 42 mezzanine location.

Figure 1: XMC-109 Processing Architecture





Dual Core Freescale Power Architecture QorIQ P2020 PowerPC

The processing function of the XMC-109 is powered by the QorIQ P2020. The P2020 SOC includes the following functions and features used on the XMC-109:

- Two e500 Power Architecture cores
  - Shared 512KB L2 Cache with ECC
  - 32KB L1 instruction and 32KB L1 data cache
  - Independent boot and reset
- Two GbE controllers
- Single 64-byte DDR3 SDRAM memory controllers with ECC
- Multi-core Programmable Interrupt Controller
- One I2C controller and one eSPI controller
- Two UARTs
- Two 4-channel DMA engines
- Enhanced local bus controller (eLBC)
- 2 PCI Express (PCIe) 1.0 controllers

If required, the XMC-109 can also support the use of a P2010 processor.

Double Data Rate (DDR3) SDRAM

The XMC-109 has one DDR3 memory controller supporting a single bank of DDR3 SDRAM. The XMC-109 may be fitted with 2 GB, 4 GB or 8 GB of DDR3 SDRAM. The DDR3 interface operates at a rate up to 800 MT/sec.

To preserve data integrity, the SDRAM controller is equipped with ECC circuitry that detects and corrects all single-bit data errors, detects all double-bit errors, and detects all 1-bit and 2-bit errors within the same nibble.

NOR Flash Memory

The XMC-109 is available with 256MB of NOR flash memory. The flash will retain data for 20 years at +85°C, assuming that the sector containing the data has less than 1,000 erase cycles. The data retention drops as the erase cycle count increases. After 10,000 cycles, data retention is for 10 years. After 100,000 cycles, data corruption will likely be noticeable in one year. Read performance of the flash array is optimized in order to minimize system boot up time for applications such as avionics mission computers where fast restarts after power interruptions are critical.

For absolute security against inadvertent flash programming or corruption, a hardware jumper is provided to disable writing to flash. The CW U-Boot of the XMC-109 provides flash programming functions with support for downloading flash images over Ethernet. See the XMC-109 U-Boot user manual for details.

NAND Flash

The XMC-109 can be optionally configured with 8GB of SATA NAND flash through a SATA interface. The NAND is equipped with a NISPOM compatible built in memory sanitation (sanitization) feature.

Permanent Alternate Boot Site (PABS)

PABS provides a backup boot capability in the event that the U-Boot in the main flash becomes corrupted. This can occur because of an error during reprogramming or an incorrect image being loaded. PABS provides users with a convenient mechanism to recover from corruption of the main NOR flash without removing the card from the system in which it is installed. An on-board jumper and a backplane signal (ALT_BOOT) are provided to cause the card to boot from PABS, thus allowing a user to reinstall the standard U-Boot load. The PABS feature guarantees that a card will never need to be removed from a system to perform NOR flash updates.

FRAM

A Ramtron FM22L16 Ferroelectric Random Access Memory (FRAM) provides 512KB of fast, non-volatile storage of mission state data that must not be lost when power is removed. FRAM reads and writes like standard SRAM and as with all FRAM devices, writes occur at bus speed and are immediately non-volatile. The FRAM memory is non-volatile due to its unique ferroelectric memory process which means that data is retained after power is removed. It provides data retention for over 10 years. Fast write timing and high write endurance make FRAM superior to other types of memory. The FM22L16 includes a low voltage monitor that blocks access to the memory array when VDD drops below a critical threshold. The memory is protected against inadvertent access and data corruption under this condition. The device also features software-controlled write protection.



Non-volatile Memory Security

The XMC-109, as well as other Curtiss-Wright Continuum Architecture products, provides for the management of non-volatile memory devices in classified circumstances. All of the non-volatile devices, flash, PABS flash, FRAM and FPGA PROM may be individually write-protected by a hardware jumper. The jumpers may be visually inspected to conform to security procedures. The CW U-Boot of the XMC-109 provides non-volatile sanitization functions to perform a secure erase per NISPOM requirements.

The XMC-109 I/O System

The XMC-109 features a large number of I/O interfaces including EIA-232/EIA-422 serial ports, USB, Ethernet, SATA and LVTTL discrete I/O. All major I/O for the card is placed on 40 signal pins such that they can be accessed on a basecard that provides an XMC site pinned out to VITA 46.9 X8d+X12D or X12d+X8D of the PN6 connector. Other signals are available on single ended XMC signal pins.

Gigabit Ethernet Interface

The XMC-109 is equipped with up to two 10/100/1000Base-T Ethernet interfaces, both implemented within the P2020. The Ethernets are autonegotiating and can be factory configured for 1000Base-X operation. The Ethernet controllers integrate a number of features designed to minimize processor loading due to Ethernet traffic. These include dedicated DMA engines, support for jumbo packets up to 9 KB, efficient buffer management schemes, checksum calculation for IP, TCP, and UDP, and interrupt coalescence.

Serial ATA (SATA) Interface Option

The XMC-109 optionally provides one SATA 2.0 port on the PN6 connector. (Note: when equipped, the PCIe fabric on Pn5 is reduced to two lanes)

Two EIA-232/422 Serial Ports

All XMC-109 configurations have two EIA-232/422 serial channels. These are routed to the PN6 connector. The EIA-232 serial ports support asynchronous communications with one transmit and one receive signal. One serial port supports a cable detect pin to automatically detect the connection of a cable which can be used to control the boot-up sequence of the card if desired. The two serial ports are implemented with the P2020's DUART. The baud rate of two ports can be set independently from 300 to 115200 KBaud.

LVTTL Discrete Digital I/O Option

The XMC-109 provides 4 bits of LVTTL compatible discrete digital I/O. Each bit is individually programmable to be an input or output and is capable of generating an interrupt upon a change of state, with programmable edge detection. The output drive current is 24mA.

One USB 2.0 Port

The XMC-109 provides one USB port from the P2020 that goes through a USB driver to the PN6 connector.

The port provides a +5V output to power external USB devices such as keyboards.

Extensive Timing Resources

The XMC-109 provides a large number of timing resources to facilitate precise timing and control of system events. The list of available timers is shown in Table 1.

Real-Time Clock (RTC)

A Maxim/Dallas Semiconductor DS3231MZ+ RTC chip provides the RTC function. It contains registers for century, year, month, day, hours, minutes, and seconds. The RTC is capable of generating alarm interrupts. The RTC draws its power from VPWR and in the event of loss of power, the RTC will automatically switch over to draw power from 3.3V_AUX.

Avionics Watchdog Timers

The XMC-109 provides two watchdog timers. Each watchdog timer is a presettable down-counter with a resolution of 1 µsec. Time-out periods from 1 msec to 33 seconds can be programmed. Initialization software can select whether a watchdog exception event causes a software interrupt, a processor reset, or a card reset. Once enabled to cause a reset, the watchdog cannot be disabled. A watchdog event indicator discrete signal is output to the backplane.

The watchdog timer can be used in two ways. As a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register. For increased system integrity, the watchdog can optionally be configured to operate in “Avionics” mode whereby a minimum interval between writes to the watchdog register is also enforced. In other words, writing to the watchdog register too soon or too late causes an exception event.



Table 1: XMC-109 Timing Resources

Timer	Implementation	Type	Size	Tick Rate/Period	Maximum Duration
PowerPC Time Base Register	One per CPU	Free Running Counter	64-bit	37.5 MHz/26.67nsec	
PowerPC Decrementer	One per CPU	Presettable, readable downcounter	32-bit	37.5 MHz/26.67nsec	34.35 sec
General Purpose #0-7	P2020	Presettable, readable downcounter with auto-read and stop options, divide by 8, 16, 32 and 64	31-bit	37.5 MHz/26.67nsec (default)	57.26 sec
RTC Alarm	RTC	Alarm Interrupt	-	1 Hz/1 sec	200 years
Watchdog Timers	Core Functions FPGA	Presettable, readable downcounter with interrupt or reset on terminal count	25-bit	1 MHz/1usec	33.55 sec
System Timers #1-6	Core Functions FPGA	Presettable, readable downcounter with interrupt on terminal count	32-bit	50 MHz/20nsec	85.9 sec

General Purpose DMA Controllers

The P2020 provides two 4-channel DMA controllers that are available for general purpose use. The DMA controller can be used for transferring blocks of data between the SDRAM, flash memory, device bus peripherals, and the PCI busses. Direct and descriptor-driven chained operation are supported, as are source and destination striding. The DMA controllers also feature a bandwidth management feature to allow the user to control the distribution of bandwidth between the four DMA channels.

VITA 42 XMC

The XMC-109 is designed to VITA 42.0 and 42.3. When installed on a conduction-cooled carrier/basecard, the XMC-109 adheres to the VITA 20-2001 (R2005) conduction-cooled PCI Mezzanine Card (PMC) standard specifications. The XMC-109 can also be configured with VITA 61 connectors. Please contact the factory for details.

The XMC-109 uses both the Pn5 and Pn6 connectors for interface to the carrier card. All I/O is on the Pn6 connector.

I2C and eSPI Ports

The XMC-109 supports a single I2C port directly off the P2020 to the Pn5 connector which can be configured to:

- act as a slave where devices are read from an external controller,
- or as a master when the XMC-109 is acting as the main processing node in the application.

The XMC-109 also supports a single eSPI port directly off the P2020 to the Pn6 connector.

PCIe Interface

The XMC-109 has 4 lanes of PCIe Gen1 direct from the P2020 to the PN5 connector. These are pinned out as per VITA 42.3. The lanes can be configured as follows:

- single x4 lane port that can operate as a root node or end point
  - available only when NAND FLASH or SATA is NOT installed
- two x2 lane ports that can operate as root nodes or end points
  - both need to be similarly configured
  - available only when NAND FLASH or SATA is NOT installed
- single x2 lane port that can be operate as a root node or end point
  - available when NAND FLASH is installed
- other combinations are possible. Please consult factory.

The conduction-cooled XMC-109 adheres to the VITA 20-2001 (R2005) conduction-cooled PCI Mezzanine Card (PMC) standard specifications.

Debug Interfaces

For debugging purposes, the XMC-109 has made allowance for a COPS debug connector to be mounted on to the mezzanine. Consult the factory for details.

The XMC-109 also responds to the MRSTI# signal on the Pn5 connector driven by the carrier card.

Temperature Sensors

The XMC-109 provides two sensors to measure board and processor temperatures. One is placed near the card edge, and the other measures the CPU temperature.

Designed for Harsh Environments

The XMC-109 can be used on air-cooled and conduction-cooled carriers/basecards. The operating conditions are dependent on the application and cooling method.

For air-cooled environments, the amount of air flow required to adequately cool the XMC-109 is dependent on the application, inlet temperature, and basecard used. Consult the factory for advice on operating in a rugged air-cooled environment.

When used on a conduction-cooled carrier/basecard, the XMC-109 is designed to make use of both primary and secondary mezzanine cooling interfaces. If used on a standard XMC site with a mid plane, the XMC-109 is designed so that the processor can be padded to the mid-plane to provide adequate cooling and so that all devices are within their maximum junction temperature. Improved results can be obtained with a customized metal frame designed to reduce the gap between devices and the frame. Consult the factory on advice and details for designing an optimized cooling solution.

Software Support

Curtiss-Wright's suite of U-Boot and BSP APIs is common to other SBCs (VME and VPX) multi-processor boards. Developers of mixed systems will find a common set of features and software interfaces for all future processing products from Curtiss-Wright.

U-Boot Monitor

The monitor provides a command line interface over a serial port or Ethernet to allow a user to perform a variety of system integration activities with the card. The monitor provides debug and display commands, diagnostic results display and exerciser controls, non-volatile memory programming and declassification and programming of parameters used to control boot-up and diagnostics.

Built-in Test (BIT)

BIT is a library of diagnostic routines to support Power-up BIT (PBIT), Initiated BIT (IBIT), and Continuous BIT (CBIT) designed to provide 95% fault coverage.

Operating System Software

The XMC-109 is supported with an extensive array of software items, which cover all facets of developing application code for the board. Users have the option of choosing to develop with a variety of operating systems and development tools. The following operating systems are supported or planned for the XMC-109:

- Wind River VxWorks 6.9+ SMP Workbench 3.3
  Part Number: DSW-109-0106-CD
- Wind River Linux (4.3)
  Part Number: DSW-109-6400-LNX

Power Consumption

See Table 2 for power consumption for the XMC-109 standard product variant. Power consumption increases as operating temperature rises.

The XMC-109 is designed to run off VPWR which can be 5 to 12V and does not draw current from the other voltage rails for normal operation. Hence, power consumption in the table below is for 5V only. Contact the factory for other configurations.

FPK-109-000

For development purposes, a front pack adapter can be ordered to be used to obtain access to the majority of signals on the VITA 42 Pn6 connector. This allows the card to be used on any base card that supports a PN5 connector. Consult factory for details.

Figure 2: Front Pack 109 Adaptor

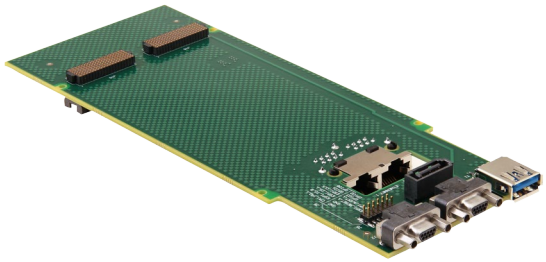




Table 2: Variant Power Requirements

Ruggedization Level	Part Number	Reference Configuration	Max Typical Power (W)
Level 200 Conduction-cooled	XMC-109-C2000	• P2020 • 2GB DR • 256M NOR • 8GB NAND • 2x 1000Base-T GigE • 2 EIA-232/422 • USB • SATA • DIO • ePSI	18
Level 200 Conduction-cooled	XMC-109-C2001	• P2020 • 2GB DR • 256M NOR • 2x 1000Base-T GigE • 2 EIA-232/422 • USB • SATA • DIO • ePSI	15

Note: Typical power is measured power while running stress test software that exercises CPU and board functions. The actual power consumption observed will vary by application.

Table 3: Typical Maximum Current Requirements

Voltage	Ruggedization Level	Max Typical Current Amps	Comments
+5V (VPWR)	Level 0	TBD	
	Level 200	3.6 (TBC)	
+3.3V	All levels	0	Not used
+/-12V	All levels	0	Not used

Note: For thermal design considerations, Curtiss-Wright recommends adding 5% to the typical power consumption. For power supply sizing, Curtiss-Wright recommends adding 20% to the typical power consumption.

Specifications

The XMC-109 standard product is produced as a lead free assembly. A tin-lead assembly can be provided as a customer specific variant.

Table 4: XMC-109 Dimensions and Weight

Option	Dimensions	Weight (grams)
Air-cooled Level 0 and 100	per VITA 42	90
Conduction-cooled	per VITA 42	95

Table 5: XMC-109 Cooling Requirements

Configuration	Temperature Range	Air Flow (CFM)
P2020 up to 1.2 GHz	-40 to 71°C	12

Notes: Air-flow is specified for sea-level conditions. The temperature refers to the inlet temperature at the card. The air-flow specifications are for worst case (highest power) conditions. Curtiss-Wright can supply additional recommendations for specific power/temperature/altitude scenarios and pressure drop characteristics to support the design and testing of cooling subsystems.

Ruggedization Levels

Air-cooled cards are available in Levels 0 and 100.

Conduction-cooled cards are available in conduction-cooled Level 200. See the Curtiss-Wright Ruggedization Guidelines fact sheet for more information.



Ordering Information

The XMC-109 is ordered with the following part numbers. Not all possible configurations are offered. Consult Curtiss-Wright for available configurations.

Options in yellow will be available as standard product with following limitations:

- Contact the factory for other variants
- All others available as customer specific variants with CM Service

XMC - 109 - ctxyy

I/O Mode:
- 000: P2020, 2GB DR, 256M NOR, 8GB NAND, 2x 1000Base-T GigE, 2 EIA-232/422, USB, SATA, DIO, ePSI
- 001: P2020, 2GB DR, 256M NOR, 2x 1000Base-T GigE, 2 EIA-232/422, USB, SATA, DIO, ePSI
- 002: P2020, 2GB DR, 256M NOR, 8GB NAND, 2x 1000Base-X GigE, 2 EIA-232/422, USB, SATA, DIO, ePSI
- 003: P2020, 2GB DR, 256M NOR, 2x 1000Base-X GigE, 2 EIA-232/422, USB, SATA, DIO, ePSI
- 9xx: Custom variant

Ruggedization Level:
- 0: L0 (0 to 50°C)
- 1: L100 (-40 to 71°C)
- 2: L200 (-40 to 85°C)

Cooling Method:
- A: Air-cooled
- C: Conduction-Cooled

Model Number: 109

Form Factor: XMC

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:

Website: www.cwcdefense.com/sales

Email: ds@curtisswright.com

Technical Support

For technical support:

Website: www.cwcdefense.com/support

Email: support@curtisswright.com

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