Case Study

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DIGITAL RECEIVER SYSTEM for Multi Object Tracking RADAR (MOTR)

Introduction

The MOTR is a sophisticated Monopulse Pulse Doppler RADAR used for tracking satellite launch vehicles and space debris. This RADAR uses modern processing techniques to extract target range, position and velocity. While the theory of operation has not changed over the years, there have been considerable improvements in the implementation of RADARs. Most notably, implementation of Digital Signal Processing (DSP) algorithms has moved from large computers to a single notebook-sized Single Board Computer (SBC).

The MOTR consists of the following sub-systems:

- Phased Array antenna.
- RF Down Conversion.
- Digital Receiver System (DRS)
  - Processing of the raw signal returns and detection of targets.
- Data Processing System (DPS)
  - Scheduling of scan operations and tracking of objects.

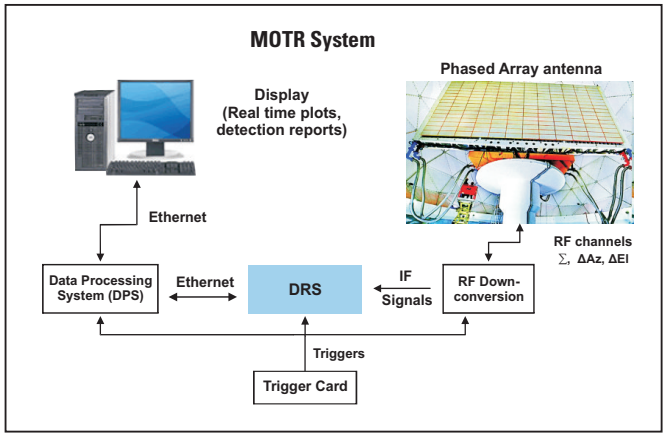
> "This case study showcases Mistral's expertise in High Performance Embedded computing and Hardware/Software/ FPGA co-design"

The Requirement

The customer Indian Space Research Organization (ISRO) required Mistral to jointly work with them to develop a Digital Receiver System for their Multi Object Tracking RADAR (MOTR) that would provide good dynamic range and complete processing of the target returns every Pulse Repetition Interval (PRI).

The DRS is a RADAR Signal Processor (SP) which is capable of extracting signal information from raw radar returns in real-time. The performance of the RADAR is limited by the amount of processing that can be handled by the DRS.

Here's a look at the setup and configuration of the MOTR system.

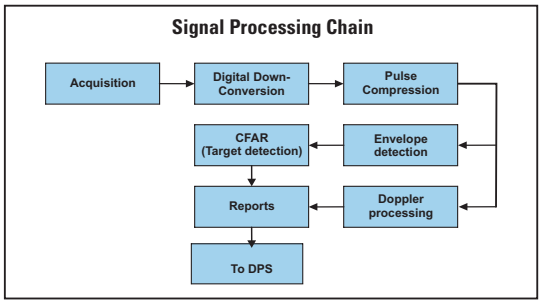


The following list enumerates the functions of the DRS, which are typical of RADAR receivers.

- Coherent acquisition of IF signals.
- Calibration and diagnostics.
- Digital Down Conversion with programmable bandwidths and decimation rates.
- Fast Pulse compression using FFT. The maximum FFT length supported is 512k samples which corresponds to a range gate ~ 1000kms.
- Coherent/Non-coherent integration.
- Automatic target detection using CFAR techniques.
- Velocity estimation using Doppler processing.
- Data logging of intermediate processing results for diagnostic purposes.

Solution Provided

The DRS is a critical part of the MOTR. It is a high-performance signal processing platform which is used to accelerate time-consuming algorithms and perform real-time target detections. The detected target reports are sent to a Data Processing System (DPS), over Gigabit Ethernet, for further analysis, classification and tracking.



In order to meet the stringent processing requirements, Mistral recommended a COTS VPX based Hybrid computing platform with a Dual Core PowerPC processor and two Xilinx Virtex-6 SX series FPGAs. The FPGAs are used for accelerating the signal processing and detection algorithms. All processing was done using IEEE-754 single precision floating point arithmetic.

The processors were used for control of sub-systems, calibration and diagnostics, generation of reports to be sent to the DPS.

Mistral developed an advanced system comprising of the following components:

- DRS embedded software.
- DRS FPGA logic.
- Graphical User Interface.
- 19" VPX rack mountable chassis with power supply unit.
- A COTS VPX based computing platform featuring
  - Dual Core PowerPC processor.
  - Two high-end Xilinx Virtex-6 DSP family FPGAs.
  - SRIO Interconnect.
- Two COTS FMC based acquisition modules for Analog-to-Digital conversion of IF signals.
- One COTS clock distribution module.

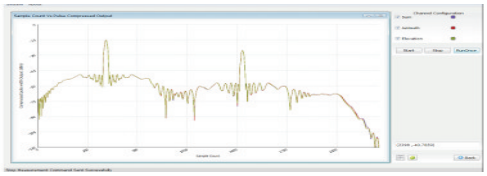
The Challenges

- The customer wanted a highly-configurable system with provision for supporting different processing techniques.
- Implementation of a large pulse-compression filter using hyper-length FFT. Since the pulse compression filter consumes a significant portion of the available computation time, it was imperative to design an optimal FFT specific to the platform.
- Computation time restricted to 1 PRI
  - Failure to complete processing in time results in loss of target information.
  - Failure compromises the accuracy and stability of the system.
- Floating-point implementation of CFAR algorithms (CA, OS and variants) with the facility to use all detectors in parallel with a computation time of O(N).

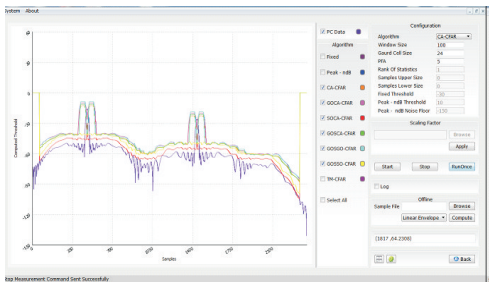
Key Achievements

- Highly pipelined floating point design to meet the computation time deadlines.
- Development of an optimized Digital Down Converter (DDC) to supports decimation rates of 2 - 63 in integer steps.

Real-time display of pulse compression filter



Offline analysis of target detection techniques



- Hyper-length FFT with a complexity O(2N) compared to traditional implementations with a complexity of $O(N \log_2 N)$.
- High-performance floating-point CFAR engine with support for CA/GOS techniques with a computational complexity of O(N).
- Excellent support for offline analysis
  - Antenna pattern measurement.
  - Automatic calibration and diagnostics.
  - Analysis of detection performance of target detection algorithms.

Customer Benefits

- A multi-vendor selection of best-of-breed sub-systems was made available as an integrated system through a single system integrator; who not only provided the solution but would also provide support and maintenance for the coming years.
- Shortens customer's end-to-end product development cycle and ensures on-time deployment schedule.
- Leveraging Mistral's expertise in High Performance Embedded computing and Hardware/Software/FPGA co-design, we were able to deliver a fully integrated deployable solution.

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