WHITE PAPER

Layout Challenges in High-speed Mixed Signal Design

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Introduction

With Telecom Revolution at peak, designing systems at higher and higher operating frequencies has become the need of the hour. Though this sounds very simple it brings along numerous design issues an engineer has to face and resolve. The issues become even more critical when it is a mixed signal design, i.e., a design with both analog and digital components and interfaces between them. The paper discusses mainly the challenges in a high-speed mixed signal design, their cause and the means to minimize their effect on system performance and reliability. The paper also presents a case study and results in support of the suggested design methodologies.

The Challenge

In high-speed mixed signal designs, the biggest challenges are achieving good sensitivity over wide dynamic range and fidelity. In other words, it is obtaining good signal to noise ratio (SNR) and faithful reproduction of system performance at any time.

The main factors influencing the system performance are

1. Switching noise
2. Cross talk
3. Quality of on-board clocks
4. Operating temperature
5. Ground Loops

Switching Noise

Switching noise is unavoidable in mixed signal designs. One major reason for switching noise is high to low or low to high voltage level transitions on the board. These transitions trigger a high instantaneous current requirement which leads to ground bounce. There are two important sources of this noise.

1. Simultaneous Switching I/Os -Digital devices with high-speed switching I/Os
2. On-board clocks

Another significant contributor to the switching noise is the switching regulators on the board. They primarily contribute noise in the lower end of the frequency spectrum

Cross talk

Crosstalk is the unwanted coupling of the signals. The coupling is caused by either conduction or radiation. Faithful and consistent performance in high-speed system is achieved by minimizing the crosstalk.

Effects of Crosstalk become more prominent with higher operating frequencies.

The sources of crosstalk are conduction, capacitive and indutive couplings between the signals.

Conduction Coupling

The conduction coupling happens through copper. It occurs because of the common interface between the devices and the ground. Whenever a signal is connected to two devices the noise coupled to one device travels to the other through the copper trace of that signal.

Capacitive Coupling

In capacitive coupling, a voltage change in one trace impacts another trace due to physical proximity of the two traces.

The two traces running parallel and closer to each other, with the dielectric between them forms the capacitive effect. The traces either running parallel to each other in the same layer or on top of each other in adjacent layers will cause this coupling. This capacitive coupling can be avoided by providing proper ground between the signal traces.

Inductive coupling

Radiated coupling occurs when the electro-magnetic field from one trace induces a signal in another trace. One of the primary causes for this coupling is the lack of nearby ground reference for high speed lines. In this case, signal travels on the periphery of the trace due to skin effect. It tries to find a path to ground through an adjacent trace since a ground cannot be found. In addition, any ringing in the digital signals will cause

radiation. This radiation can couple on to the board if another trace happens to present the correct conditions (such as impedance, polarization, etc).

Quality of on-board clocks

The quality of clocks generated on board also plays a major role in the system performance. The aim is to achieve a jitter free clock with good rise time characteristics. One of the key factors affecting clock characteristics is clock circuit placement and routing.

Temperature

Faster the switching rate higher the heat dissipation from the device. This can lead to high temperature zones on the board. It affects the performance of sensitive analog components. Also the fidelity and lifetime of the system becomes questionable. Hence the layout of critical analog and clock components becomes a challenge in itself. It is imperative to avoid the placement of these components near thermally hot zones on the board.

Ground loops

Always it is spoken that lot of care should be taken in the ground connection of mixed signal board. Usually the analog and digital grounds are separated and joined at only one place, but the cross over of signals between analog and digital components is ignored. It leads long ground return paths to the signals. While this in itself is a major problem, it is often compounded by the inadvertent presence of another ground return path. This is called a ground loop.

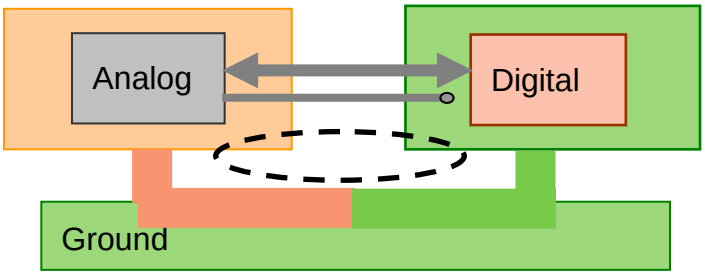

Figure 1: Ground loops

If the ground loop length is comparable to the rise time of the switching signal it acts as an antenna. This antenna can couple or radiate unwanted noise to the signals in the same board and adjacent boards.

Our Approach

In order to design a system with good sensitivity and fidelity, we took a two-tier approach.

1. Design
2. PCB layout and Routing

Design

The design involves the selection of components and the implementation to achieve the requirements.Choosing the correct component is achieving half the goal. In high-speed designs using differential components is very essential since it minimizes the effects of crosstalk and switching noise. The various analyses like timing, ac load, power, temperature and decoupling are done in the design level. The timing and ac load analyses help to identify the rise time issues between the components.The temperature and power analyses help to identify the high-heat dissipating components. This plays the key role in placement.Decoupling analysis is performed to select suitable capacitors to minimize the effect of switching noise.

Layout and Routing

Layout and routing is an art by itself. Sufficient thought has to be put in order to get the best layout of the design. It becomes even more challenging for high-speed mixed signal design. The issue here is handling the coexistence of analog and digital components and the interfaces between them. The placement is done to avoid the digital switching noise coupling to analog signals. The routing strategy is to minimize the crosstalk and to maintain the good quality of signals and clocks across the board. The routing theme also takes care of signals crossing domains.

PCB layout or Placement

(i) Analog and Digital separation

As discussed before the separation of analog and digital components in placement becomes essential to reduce digital switching noise interference.

(ii) Clock Section

In any design all the clocks should be synchronized to a common source to achieve good performance. In mixed signal design both the analog and digital components have to use the same clock source. This leads to noise coupling from digital components to analog components through clock. Hence more care should be taken in clock circuit placement and clock routing.

Also the placement of the clock components needs to ensure the shortest path between source and destination. It prevents the clock from distortion and provides for a low jitter distribution.

(iii) Power Section

In power design linear regulators are used for analog components to avoid noise. Switching regulators, being more efficient are used for digital components.

The criteria of placement are to keep these power supplies closer to their respective domain and farther from each other. However, the problem is complicated by the fact that usually the power to the linear regulator is supplied from one of the switching regulator.

(iv) Layer Stack Up

The layer stack up is governed by the number of power rails and signals to be routed. In addition stringent placement requirements may call for additional layers.

In high-speed mixed signal designs the top and bottom layers are filled with ground. It shields the board from radiated interference. Another good effect of

this practice is the additional surface area for thermal conduction which helps in reducing hot spots on the board.

(v) PCB Signal Routing

Some common thumb rules for routing in a high speed mixed signal board are listed below.

- The Analog and digital signals are routed as far away as possible from each other
- Analog and Digital grounds are separated and joined in the PCB at only one place
- Switching signals and clocks are shielded by ground to avoid radiating noise
- Cross over of analog and digital signals are minimized
- Sharp edges of the PCB tracks are avoided to reduce pickup and radiating noises
- The differential signals are routed to have matched length and impedance
- Adjacent differential pairs have ground shielding between them
- For RF signals the traces should be 50Ω impedance matched

In any layer the analog and digital ground planes crossing should be avoided. Otherwise it will lead to noise coupling from digital to analog ground through the capacitive effect between them.

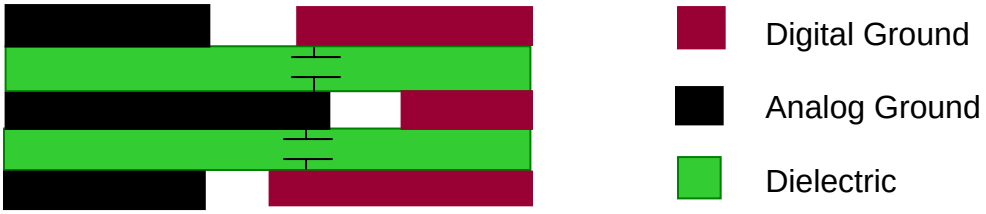

Figure 2: Ground planes crossover

The Case Study

The Digital RF Memory (DRFM) is an example for high-speed mixed signal design. It stores the RF signal in digital form and reconstructs back whenever required.
It consists of ADC and DAC operating at 600 MHz, FPGA I/Os at 300 MHz, DDR SDRAM at 200 MHz, and ADSP at 80 MHz. The RF input and output band is 400 kHz to 200 MHz.

Layout

The layout of the DRFM board is shown figure 1. It shows how the analog, clock and digital sections are placed. The care has been taken to keep the power supplies closer to the respective sections.

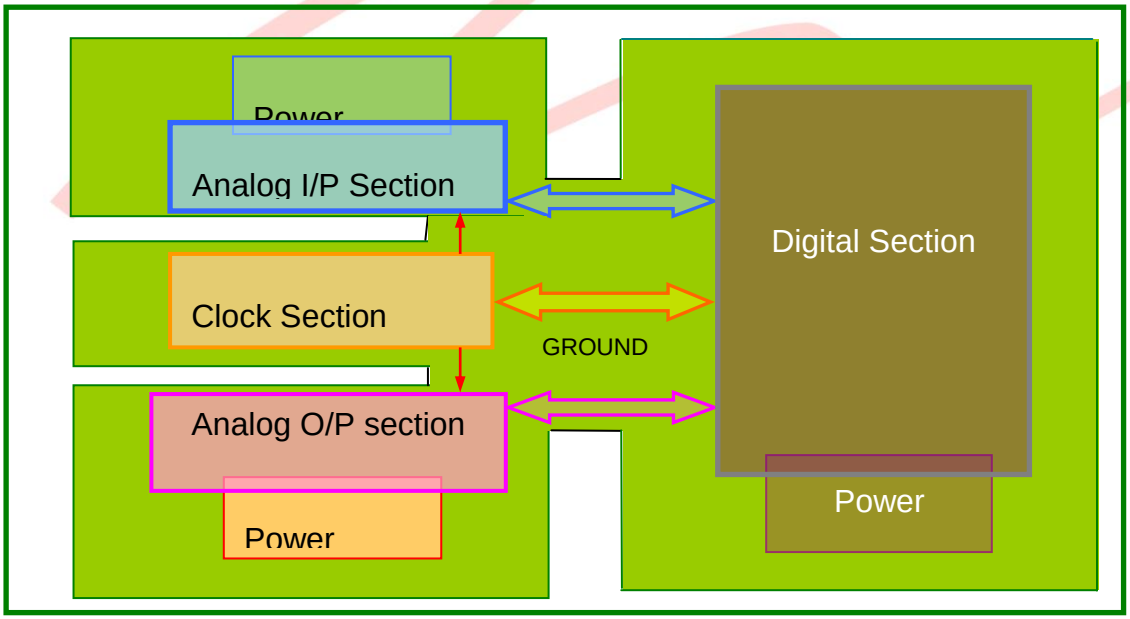

Figure 3: DRFM board layout

The analog, clock and digital grounds are shorted at only one place where the interfaces between analog and digital components happen.

The short is narrow in length and width. It provides high impedance path for high frequency switching noise in digital section to analog section.

Routing

RF signals

For RF signals routing the coplanar wave guide technique is used.

The signal trace width and the gap to ground are calculated to get the 50Ω impedance. No other signal routing is allowed in the inner layers of the RF section. The bottom layer is filled with ground.

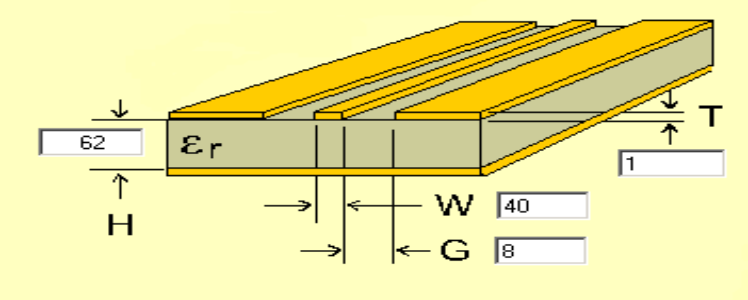

Figure 4: Coplanar Waveguide

This helps to reduce noise and crosstalk and to maintain the 50Ω impedance.

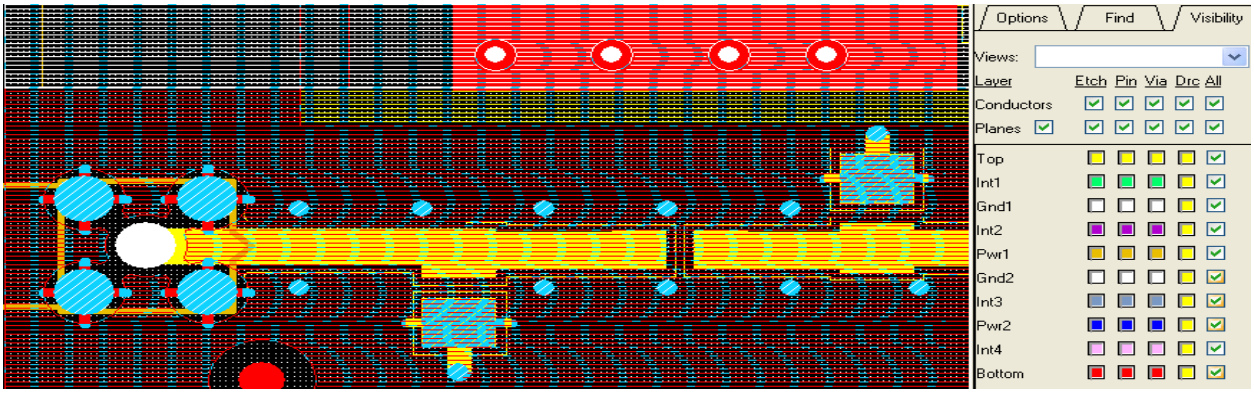

Figure 5: Snap shot from DRFM board

Differential signals

All signals above 200MHz are differential in the DRFM board. In a differential pair the traces of both the signals are length matched to the tolerance of less than 100 mils. In a device all the I/O differential pairs are length matched; tolerance between each pair is less than 500 mils. This ensures the maximum group delay of signals due to PCB trace is less than 90pS since time delay in 1inch long trace is 180pS. To reduce the crosstalk

differential pairs are guarded with ground from each other. The differential signal routing in DRFM board is shown below

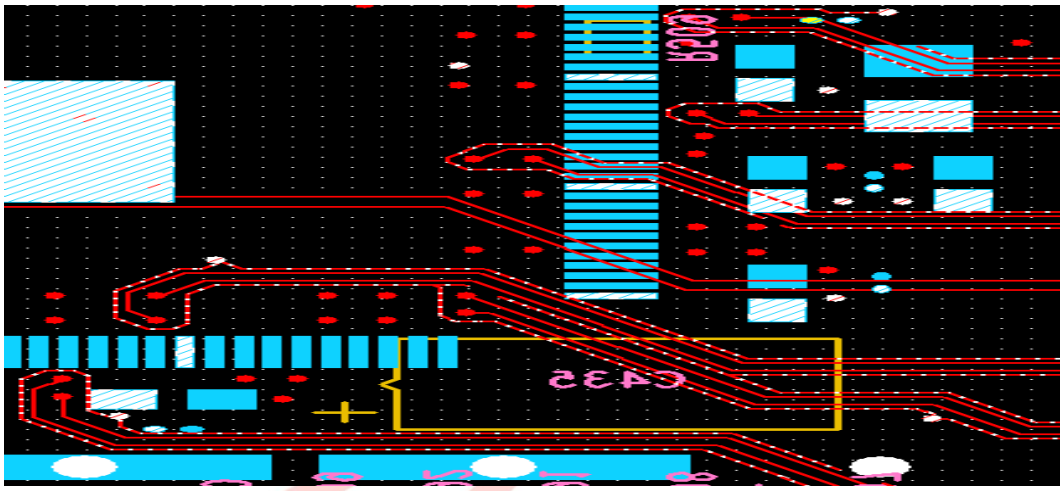

Figure 6: Differential signal Routing

Clocks

In this design all the clocks are derived from the common clock source. The common clock source can be internal PLL or external signal generator. All the clocks above 200MHz are differential. The same differential signal routing guidelines is followed for clock routing. Moreover the clock is routed with the common ground of the board to avoid ground loops. Wherever the clock has to take long path clock buffers are used

Ground separation

The grounds in the DRFM board are connected as shown in Figure 1. The analog, clock and digital grounds are shorted at only one place where the interfaces between analog and digital components happen. The short is narrow in length and width. It provides high impedance path for high frequency switching noise in digital section to analog section.

The Results

In DRFM board 8-bit ADC is used. The sampling frequency is 600MHz. The ADC capture with 50Ω termination at input shows the performance the board, the Matlab plot is shown in figure.

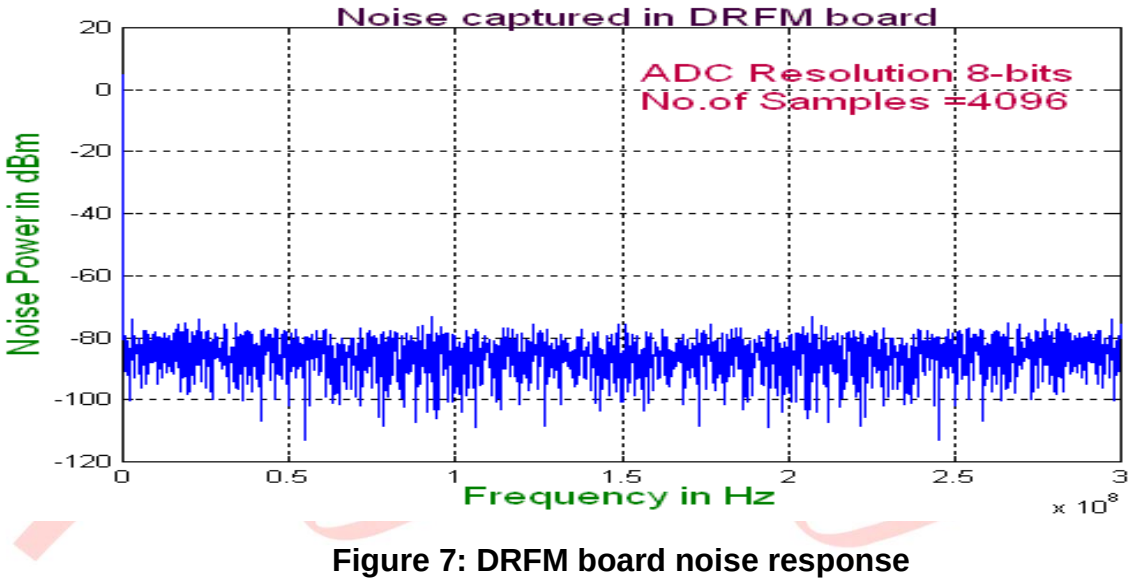

Figure 7: DRFM board noise response

The SNR of the DRFM board was measured in the following way.

1. The input was terminated with 50 ohms
2. No input signal was provided.
3. The ADC output was captured in the DSP. No. of samples = 4096
4. Matlab was used to calculate FFT.
5. After removing the DC component from the FFT the noise power was calculated.

The SNR is the ratio of known full scale power to noise power. From the SNR, ENOB was calculated

The achieved SNR is 48.32 dB

The theoretical SNR of 8-bit ADC is 49.94 dB

SNR= ENOB*6.023 + 1.76

The achieved effective number of bits (ENOB) = 7.73

Power plane Noise

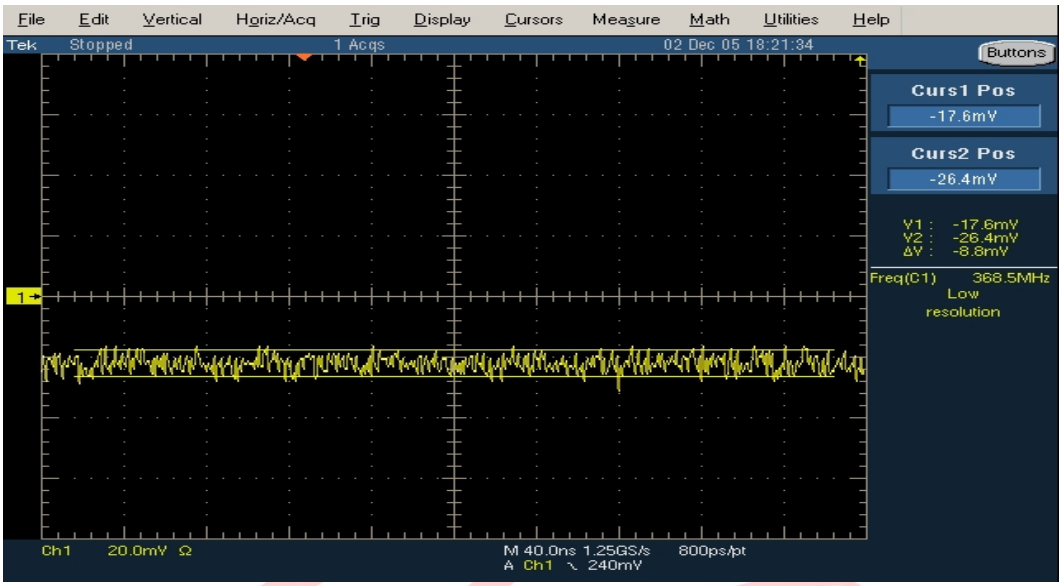

Figure 8: Power Plane Noise Captured in DRFM

The power plane noise was measured across the decoupling capacitor in the analog section while the DDR memory was accessed continuously. The noise level is less than 9mV. It was measured by using a 500 MHz, 2 GSPS oscilloscope with an active probe. The noise floor of the oscilloscope is less than 6mV.

Conclusion

The factors affecting system performances like switching noise and cross talk are well-known in the industry. It is very important to have a practical understanding of these issues to work in high-speed design. The paper intends to convey the proven high-speed design approach and the results. The paper has highlighted the causes of switching noise and crosstalk. Following the methods suggested in layout and routing of the design help to minimize them.

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- Networks, Lines and Fields by John D Ryder

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Mistral – Corporate Profile

Mistral is a technology design and systems engineering company providing end-to-end solutions for product design and application deployment. Mistral is focused in two business domains: Product Engineering Services, Defense & Homeland Security. Mistral provides total solutions for a given requirement, which may include hardware board design, embedded software development, FPGA design, systems integration and customized turnkey solutions.

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