Central Computer, Battery Pack and other accessories

The military has long needed computers that are tough enough on the outside to withstand the rough and tumble of the battlefield and secured on the inside. Now, with the proliferation of smartphones and tablets, ruggedized and secured versions of these would be in use. As soldiers would use these smartphones and tablets for their personal use as well away from the warfront, military applications will sit side by side with games and social networking apps and the devices have to be super secured.

> **"Wars and national-building activities along with terrorist threats requiring counter-insurgency in urban warfare have resulted in high demand for such modern electronics gear."**

Energy required for all the electronics carried by the soldier has to be optimized as the battery pack is the most significant component of the weight he has to carry. Batteries needed to power radios and other electronic gadgets account for a fifth of the total weight carried by soldiers. Effective battery management, low power electronics, sleep mode on systems to optimize power usage are hence a must. Creating wearable power systems and higher-voltage batteries that would require less recharging are the technologies that are being investigated. Engineers are also investigating the concept of clothing materials that can act as an electrical bus shifting power around the uniform as needed.

Conclusion

The advancement in semiconductor technologies leading to "state of the art" solutions from companies like Analog Devices Inc., are a significant contributor to enabling the levels of performance needed to meet the challenges referred to above. By making devices smaller, less power hungry, more integrated and most importantly affordable is driving Soldier electronics modernization. Wars and national-building activities along with terrorist threats requiring counter-insurgency in urban warfare have resulted in high demand for such modern electronics gear.

Trends and Challenges in Mixed Signal Designs

By Rajaram Shastri, Senior Architect, Mistral Solutions Pvt. Ltd.

Designers working on next-gen designs must intermix and deal various RF devices, data converters and complex digital circuits. As clock speeds increase, voltage levels reduce and circuit sizes shrink, engineers must address the analog behavior of digital components. Market trends force IC manufacturers to high-level integration by putting RF, analog and digital circuits in a single package. This in turn, forces designers to address mixed signal systems like never before. This article tries to address these issues at a high level.

What is Mixed Signal Design?

There is no straightforward answer. A digital design engineer may not worry about the analog nature of the signal, but as frequency increases and voltage level decreases, he mst worry about signal rise time, slew rate, offsets, coupling issues, impedance matching and measuring instrument parameters like bandwidth, termination, coupling etc. The situation is different for an analog engineer. High level of integration of PLLs, mixers, attenuators, detectors, with digital control and digital output have complicated the issues of power supply and ground isolation, return-path issues, logic level compatibility and drive strength.

ADC and DAC designs add to the complexity and designers must apply mixed signaldesign techniques for every single device on board to successfully integrate them. The high degree of integration means designers must address thermal issues of various ICs such as ADC, DAC, PLL/VCO, clock buffers and mixers. Removing hot spots from these components is critical, else performance is degraded. PCB design considerations are another aspect designers must address. Due to the high level of integration, the differentiation between RF design and analog design is very fine. Modern ICs support zero IF or low IF receivers and transmitters at various frequency bands, from S-band and going up to C-band and higher. Usage of these ICs allows design of

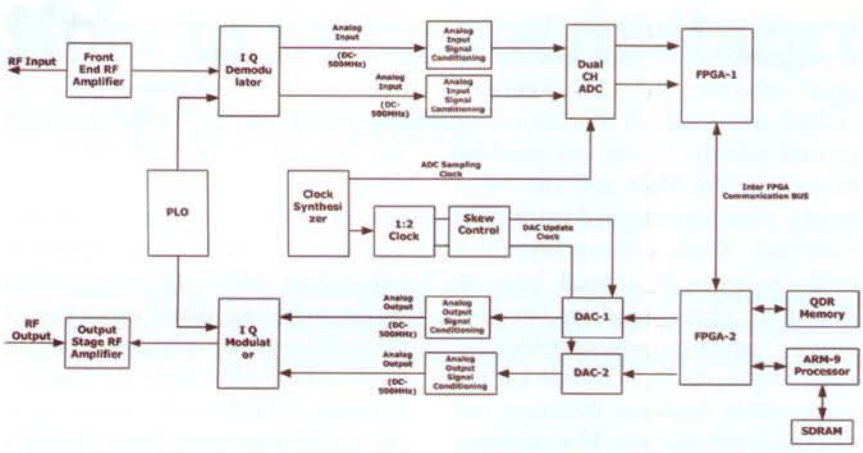

Figure 1: System Block Diagram

direct conversion transmitters and receivers. Zero IF or low IF base-band signals can be directly digitized using high-speed ADCs.

The processed base-band signal, up to 1GHz frequency can be regenerated using high-speed DACs and DDS techniques. This results in usage of complex, inter-mix of RF and data converter ICs in a single design. So designers must understand and address PCB parameters like dielectric loss, dissipation factor, skin-depth etc. The FR4 PCB material may be insufficient when frequencies increase beyond 1GHz range and other Teflon-based material may in turn be considered.

The other side of the frequency spectrum (low frequency analog design) has its own challenges.

Precision measurement of analog signals used in instrumentation and sensor design is key to any given application. ICs available in the market for such solutions are highly integrated with digital circuitry and the challenge for designers is to keep power supply noise very low, guarding analog signals from digital interferences and offset issues.

Testing and Debug

Testing and debugging is another aspect to be addressed. Digital designers must understand clock and data characteristics or differential behavior of signals. Usage of CROs with active probes and differential probes has become common and designers must understand rise-time, band-width and coupling methods of CROs and probes. Advanced triggering methods like triggering on a glitch, droop, analog level and digital cross triggering help designers debug effectively. Analog engineers must use spectrum analyzers and power meters to measure phase-noise of the clock or baseband signal power. Instrument resolution, frequency response, gain flatness and cable loss are some things to take care of when testing mixed signal designs.

Case Study

The case study here is the design and testing of 'Wideband Direct Conversion DRFM Platform', a good example of mixed signal design done by us consisting of RF, analog/data converters and high-speed digital devices. The block diagram is shown in Figure 1.

Design Challenges

- 1GHz RF Input/output Bandwidth, supporting from 1GHz to 3GHz frequency range
- In-band configurable PLO, phase noise less than -90dBc@10Khz offset
- Amplitude and phase matching of 500 MHz, base-band IQ signal
- ADC and DAC operating with 1.2GHz sampling rate
- Dual Virtex-5 SX95-T FPGAs operating at 300MHz rate
- Arm-9 processor for house-keeping and user Interface
- Conduction cooled design housed in 150mm X 130mm X 55 mm enclosure

Design Partitioning

Design partitioning is very important as this has to take care of signal flow, ease of routing, modularity,

Form -factor and thermal dissipation. It was logical to partition system functionality as RF section and digital/mixed signal section. This was realized as two separate modules as this was better suited to address thermal dissipation too.

Component Selection

The criteria selected while selecting the components was:

- The device parameters were better than the required specification
- Smallest possible footprint
- Devices should dissipate as less power as possible
- Usage of very high efficiency DC-DC converters and optimum usage of low noise, high PSRR LDOs
- Modulator and demodulator were selected such a way that they support baseband IF output with digital control for offset and carrier

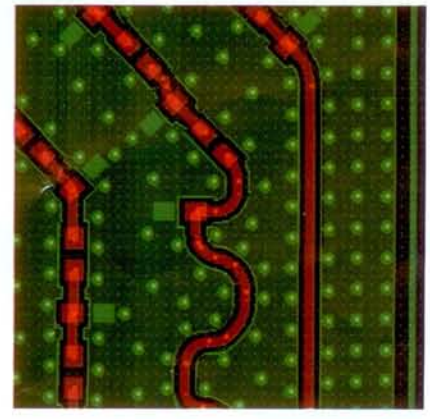

Figure 2: CPWG Routing

adjustments

- ADC selected was dual IQ ADC which supports individual gain, fullscale and offset adjustment features for each channel
- Digitally controlled PLO and clock devices
- Skew adjustment devices were added on the clock to adjust the skew or path delay between the clocks

Design and Analysis

Preliminary placement analysis was done with selected components and so the final Bill of Materials was generated with footprint, height and weight information of every component. RF path Chain Gain, Noise-Figure, input and output return loss analysis were done to ensure selected components met the required impedance matching, gain/attenuation and pass-band flatness. Loop filter values and reference clock frequency for PLO and clock synthesizer were designed for minimum phase noise output. SI and timing analysis were carried out to decide the topology for QDR-II SDRAM and inter FPGA interfaces. Power analysis and power budget analysis was carried out to decide on the power tree and thermal dissipation of the system. Thermal dissipation for each component was calculated and this value with the junction temperature data from the datasheet and junction to case thermal resistance, again from datasheet, was used for thermal analysis. 3-D thermal analysis was also carried out at different ambient conditions to identify hot spots.

Lay-out Consideration

PCB layout is the critical aspect in any mixed signal design. Proper grounding, shielding and return paths have to be provided for all the signals else the design w ll have timing, EMI /EMC or crosstalk issues. Proper PCB stack-up is the first step in lay-out. As we were dealing with signals which operate at RF range, FR4 substrate was not suitable. Top layer is designated as RF layer and the RF grade substrate, RO-4350 (alternate Nelco) was used. A discontinuous ground reference plane was provided beside the RF layer and the other layers were constructed with FR4 substrate. Every routing layer was made to refer to ground layer to eliminate cross-coupling between signals. Impedance was calculated for each routing layer to decide on the trace width, dielectric thickness and ground layer spacing. The designed PCB stack-up was verified with the fabricator so that it catered to the DFM requirements. Length matching constraints were provided for analog IQ signals, clocks and high speed digital interfaces. CPWG routing technique was adopted for RF signal routing. GND Vias were stitched for less than □/20 distance so that they acted as shields from other stray signals (Figure 2). All power nets were filled with appropriate copper width, so that trace inductance was minimized. Shielding was provided for RF sections. Finally, all ground layers were stitched with vias to provide single contiguous reference plane.

Enclosure Design

Aluminium-6061A alloy was used for enclosure fabrication and designed based on the component placement, thermal analysis data and dimensional constraints. Thermal hot spots were analyzed for maximum case temperature and as required these devices were thermally shunted to the enclosure.

Testing

After basic board bring-up test, each interface was tested for its functionality. RF Input path Ga in and flatness tested. IQ output from demodulator was tested for gain match and phase match and matched RF cables were used to probe signals on CRO. Input channels of the CRO were de-skewed before the test. If observed gain was not with-in 1dB flatness, then either digital tuning or component- level tuning of the IQ outputs individually for each channels was done to obtain flatness. Digital data from the ADC was captured and analyzed using MATLAB. The gain for each ADC input was adjusted to -1dBFS range and offset in the incoming signal was adjusted through the offset adjustment feature in the ADC. ADC data was captured through FPGA and written into the QDR-II memory. Data from the QDR-II memory was read back and written into the DAC.

The DAC output was tested for its phase and gain match using the DSO. DAC clock skew was adjusted to obtain the phase match, with in ±2°. The output of the DAC was fed to modulator and then to RF low noise gain block to adjust the output power level. After this basic testing, the RF pass-through test, RF-in to RF-out were done using signal generator and spectrum analyzer. Testing was done to characterize the undesired side-band suppression (≥30dB) and carrier suppression, (≥30dB). Initial results were 3-4dB less than desired parameters. The LO power level was then adjusted to give better carrier suppression and offset on I and Q channels were manipulated to provide the desired side-band suppression.

Finally, the system was put into the enclosure and tested for different environmental conditions.

Conclusion

This case study addresses the methodology for design and testing of mixed signal systems at the top level. Those working on such designs should be detail-oriented and have a structured approach. Detailed analysis and thorough testing is essential to get the needed performance. In any mixed signal design there is only one way to get it right, but many ways to get it wrong.