Case Study

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RF Data Acquisition Card for Direct Sampling of L-band to X-band Signals

Introduction

RF Data Acquisition Systems for wideband applications are gaining immense popularity as they are replacing the conventional RF super heterodyne receiver architecture with direct sampling architecture. These boards can directly digitize RF carriers up to X-band frequencies with an instantaneous bandwidth of 3GHz. The RF Data Acquisition Cards [RFDAC] find a wide variety of applications in Phased Array RADARs, Electronic Warfare, Signal Intelligence (SIGINT) Systems, Multi-band Diversity Digital Receivers, Satellite Communication, etc.

This case study showcases Mistral's expertise in design and development of a multi-channel RF Acquisition Card, which consists of FPGAs, ADCs, JESD204B Compliant Clock Schemes, etc. that offers unprecedented speed, signal fidelity and on-board real-time data processing – all in the smallest form-factor.

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The Customer

The customer is a leading Defence Research and Development Organization, involved in the development of avionics systems for Indian Defence.

The Requirement

The customer approached Mistral to develop a RF Data Acquisition Card [RFDAC] - 6U VPX based conduction-cooled module that adheres to VITA 46 standard, for one of the Avionics projects. The card had to digitize the incoming RF signals at a sampling speed greater than or equal to 6GSps.

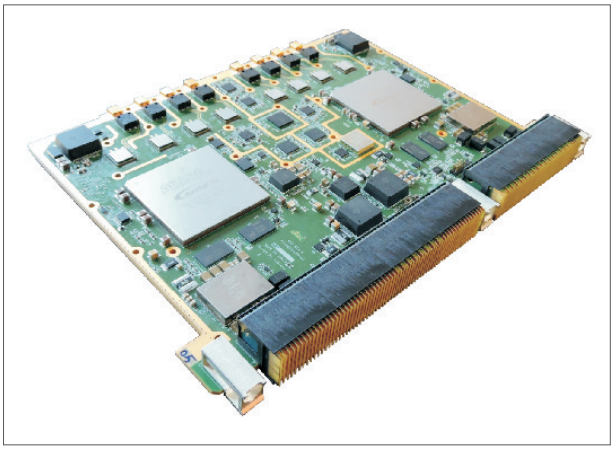
This was a build-to-spec project and the preliminary design of the RFDAC was provided by the customer. Mistral had to conduct a feasibility study of the design; and any changes / improvements in the design had to be discussed and finalised with the customer. The RFDAC development involved:

- Design architecture of the RF Data Acquisition Card.
- Schematic capture as per the final design approved by the customer
- PCB layout for RF Data Acquisition Card and the test jig [Backplane] - The boards had to meet Group A certification standards and the assembly procedure as per IPC standard
- High-speed signal simulation and analysis.
- Signal integrity, power integrity and thermal analysis
- Fabrication and bare board testing of the fabricated card and assembly as per IPC standard
- FPGA firmware and software development for all hardware interfaces
- Development of test jig for the RFDAC to test all the peripherals
- Acceptance test procedure for standalone testing of the card with test jig and host PC
- Design & fabrication of a cover-plate [Conduction-cooled heat sink plate] for RFDAC for thermal management and RF shielding
- Wedge lock mechanism to be provided to mount RFDAC.

Solution Provided

Mistral developed the Data Acquisition Card, meeting all the requirements as defined and agreed with the customer. Mistral ensured that the 6U VPX based conduction-cooled module meets all the requirements of VITA46 standard.

The board consists of Eight ADCs to digitize the incoming RF carriers simultaneously. All the ADCs are phase matched and clocked with programmable Sampling clocks. Two high-speed FPGAs acquire and process the data with necessary digital signal processing algorithms. This processed data is sent to other modules in the system using PCI Express interface via VPX backplane. The FPGAs on board are interconnected each other with a high-speed serial interface for seamless operation. The card is designed with an appropriate power section to provide power for the entire board. All the voltage rails are derived from +12V and +5V DC supplies available on the VPX backplane.



Features

RF Data Acquisition Card - a conduction-cooled 6U VPX form-factor card - is built around Intel FPGA and TI ADC. The various features of the card include

- Dual high-speed, high-density Arria-10 FPGAs
- 8 Nos of 12-bit JESD204B compliant ADCs
- Programmable JESD204B compliant clocking section
- 4 lane PCIe connection from each FPGA to VPX backplane
- Gigabit Ethernet, RS232 and RS422 serial communication links from each FPGA terminated to backplane connectors
- 2GB of DDR4 per FPGA and 64GB of NAND flash per FPGA for recording acquired data
- Hard Reset Control through firmware or external reset; soft reset through software
- Remote programming of the FPGAs via Gigabit Ethernet in addition to JTAG option
- High-speed 4 lane Serdes interconnection between FPGAs.

6U VPX Backplane

Mistral custom designed and developed a backplane [Test Jig] to test all the peripherals of the card. It is a 3-slot 6U VPX backplane designed to test all the interfaces of the RF Data Acquisition Card.

Key features of the 6U VPX backplane include:

- 10 Gbps performance
- 2 Nos of PCIe X4 Slot connectors from each VPX slot
- 2 Nos of Ethernet PHY Transceivers with RJ45 connector from each slot
- Interfaces for power, System control, UART, JTAG, Geographical Addressing, data bus and GPIO connections.

Mechanical Cover-plate cum Heat sink

Mistral designed and fabricated a cover-plate required for thermal management and RF shielding of the conduction-cooled RFDAC. The cover-plate is fitted with a wedge lock mounting mechanism.

The cover-plate is designed as below.

- 6U form-factor
- Designed and Manufactured Custom Heat Sink Plate with the latest available technology
- Operating Temperature: -40^{0}C to +71^{0}C.

Software and Firmware

BSPs, IPC Libraries and IP Cores: BSP for NIOSII Softcore processor is developed as per the Board requirements. BSP, Drivers and Libraries compatible with VxWorks 6.9 OS.

ATP software: ATP software developed to conduct functional testing of the RFDAC.

FPGA firmware: Mistral provided firmware for all high-speed data acquisition, along with peripheral interface configuration codes.

Test GUI: Mistral developed a test GUI using QT. The GUI is designed to test all peripherals of the RFDAC and capture and plot ADC test results. It is connected to the host PC (where GUI is installed) via Ethernet interface on board.

Functional Tests

Functional tests are done to test and validate the functionality of each component and interface provided in RF Data Acquisition Card. The test procedure includes following checks.

- ADC performance like SNR, SFDR, ENOB etc.
- Data Acquisition for various sampling rates up to 6GSps
- Testing of internal interfaces: High-speed SERDES communication between FPGAs, clock synthesizers programming, DDR4 and Flash read and write, etc.
- Testing of external interfaces: PCIe/GbE/RS422/GPIO's on VPX backplane.

Environmental Stress Screening

Mistral performed ESS as per MIL-STD-810G. The card was subjected to ESS as per the following tests, specification and sequence.

- Power Burn-in Test
- Pre-thermal random vibration
- Thermal cycling
- Post-thermal random vibration.

The Challenges

Extremely high Board temperature [up to 250°C]: During post layout thermal analysis, the simulation results provided very high temperature readings at certain hot spots of the board [nearly 250°C]. Mistral designed a heat sink to bring down this temperature. However, board temperature at boundary was still reaching around 160°C [Ideal temperature is 81°C].

A highly efficient thermal heat sink design became a necessity to meet the edge temperature requirement and ensure that the temperature of the FPGA and ADC components did not exceed 95°C at any point in time. Mistral designed another custom heat sink plate with the latest available technology. This heat sink transferred heat much faster from the hot spots to the card edges where the liquid coolant is flowing. This helped in maintaining the temperature within the limits.

PCB Layout and Simulation: The digitized data from each ADC is transferred to the FPGA via a 16-lane JESD204B Serial link. There are 128 high-speed JESD lanes from the ADCs to the FPGAs apart from other high-speed interfaces such as PCIe, DDR4, high-speed Serdes links, etc.

The routing of these many number of high-speed signals was a challenge due to strict length matching and space constraints. Simulation was done on all high-speed signals before the routing was finalized. The RF Data Acquisition Card was realised using high-speed PCB material [Megtron-6] and high-density layer stack up.

Achievements

- Implementation of multiple FPGAs on a single card with 8 ADCs that are independently configurable [configure different sampling rate]
- Successfully designed an extremely complex, high-density PCB that processes high-speed RF signals
- Successfully able to achieve the SNR, SFDR and ENOB parameters as specified by the ADC manufacturer
- Implementation of a custom thermal heat sink to bring down the board hot spots from 250°C to within 95°C.

Customer Benefits

- Mistral executed a critical project for the customer, needed to be completed for one of their avionics Systems
- By using the latest ADCs in the market, customer could achieve best possible signal processing capabilities
- The RF Data Acquisition Card exceeded all performance indicators and the customer could achieve superior performance for their avionics system.

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Mistral Solutions Pvt. Ltd.,
No.60, 'Adarsh Regent',
100 Feet Ring Road,
Domlur Extension, Bangalore - 560 071
Tel: +91-80-4562-1100
Fax: +91-80-2535-6444
E-mail: info@mistralsolutions.com

Mistral Solutions Inc.,
43092 Christy Street
Fremont, CA 94538
USA
Tel: +1-408-705-2240
E-mail: usa@mistralsolutions.com

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- Hyderabad
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